7. Stratix III Device I/O Features

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Stratix® III I/Os are specifically designed for ease of use and rapid system integration while simultaneously providing the high bandwidth required to maximize internal logic capabilities and produce system-level performance. Independent modular I/O banks with a common bank structure for vertical migration lend efficiency and flexibility to the high speed I/O. Package and die enhancements with dynamic termination and output control provide best-in-class signal integrity. Numerous I/O features assist in high-speed data transfer into and out of the device, including:

- Single-ended, non-voltage-referenced, and voltage-referenced I/O standards
- Low-voltage differential signaling (LVDS), reduced swing differential signal (RSDS), mini-LVDS, high-speed transceiver logic (HSTL), and stub series terminated logic (SSTL)
- Single data rate (SDR) and half data rate (HDR—half frequency and twice data width of SDR) input and output options
- Up to 132-full duplex 1.6-Gbps true LVDS channels (132 Tx + 132 Rx) on the row I/O banks
- Hard dynamic phase alignment (DPA) block with serializer/deserializer (SERDES)
- De-skew, read and write leveling, and clock-domain crossing functionality
- Programmable output current strength
- Programmable slew rate
- Programmable delay
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- Serial, parallel, and dynamic on-chip termination (OCT)
- Differential OCT
- Programmable pre-emphasis
- Programmable differential output voltage (V_{OD})

Stratix III I/O Standards Support

Stratix III devices support a wide range of industry I/O standards. Table 7–1 lists the I/O standards supported by Stratix III devices as well as typical applications. Stratix III devices support V_{CCIO} voltage levels of 3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V.

Table 7–1. I/O Standard Applications for Stratix III Devices (Part 1 of 2)

I/O Standard	Typical Application
3.3-V LVTTL/LVCMOS	General purpose
3.0-V LVTTL/LVCMOS	General purpose
2.5-V LVTTL/LVCMOS	General purpose
1.8-V LVTTL/LVCMOS	General purpose
1.5-V LVTTL/LVCMOS	General purpose
1.2-V LVTTL/LVCMOS	General purpose
3.0-V PCI	PC and embedded system
3.0-V PCI-X	PC and embedded system
SSTL-2 Class I	DDR SDRAM
SSTL-2 Class II	DDR SDRAM
SSTL-18 Class I	DDR2 SDRAM
SSTL-18 Class II	DDR2 SDRAM
SSTL-15 Class I	DDR3 SDRAM
SSTL-15 Class II	DDR3 SDRAM
HSTL-18 Class I	QDR II/RLDRAM II
HSTL-18 Class II	QDR II/RLDRAM II
HSTL-15 Class I	QDR II/QDR II+/RLDRAM II
HSTL-15 Class II	QDR II/QDR II+/RLDRAM II
HSTL-12 Class I	General purpose
HSTL-12 Class II	General purpose
Differential SSTL-2 Class I	DDR SDRAM
Differential SSTL-2 Class II	DDR SDRAM
Differential SSTL-18 Class I	DDR2 SDRAM
Differential SSTL-18 Class II	DDR2 SDRAM
Differential SSTL-15 Class I	DDR3 SDRAM
Differential SSTL-15 Class II	DDR3 SDRAM
Differential HSTL-18 Class I	Clock interfaces
Differential HSTL-18 Class II	Clock interfaces
Differential HSTL-15 Class I	Clock interfaces
Differential HSTL-15 Class II	Clock interfaces
Differential HSTL-12 Class I	Clock interfaces
Differential HSTL-12 Class II	Clock interfaces
LVDS	High-speed communications
RSDS	Flat panel display

Table 7–1. I/O Standard Applications for Stratix III Devices (Part 2 of 2)

I/O Standard	Typical Application
mini-LVDS	Flat panel display
LVPECL	Video graphics and clock distribution

I/O Standards and Voltage Levels

Stratix III devices support a wide range of industry I/O standards, including single-ended, voltage-referenced single-ended, and differential I/O standards.

Table 7–2 lists the supported I/O standards and the typical values for input and output V_{CCIO}, V_{CCPD}, V_{REF}, and board V_{TT}.

Table 7–2. I/O Standards and Voltage Levels for Stratix III Devices *(Note 1)*, *(3)* (Part 1 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
3.3-V LVTTL	JESD8-B	3.3/3.0/2.5	3.3/3.0/2.5	3.3	3.3	3.3	—	—
3.3-V LVCMOS	JESD8-B	3.3/3.0/2.5	3.3/3.0/2.5	3.3	3.3	3.3	—	—
3.0-V LVTTL	JESD8-B	3.3/3.0/2.5	3.3/3.0/2.5	3.0	3.0	3.0	—	—
3.0-V LVCMOS	JESD8-B	3.3/3.0/2.5	3.3/3.0/2.5	3.0	3.0	3.0	—	—
2.5-V LVTTL/LVCMOS	JESD8-5	3.3/3.0/2.5	3.3/3.0/2.5	2.5	2.5	2.5	—	—
1.8-V LVTTL/LVCMOS	JESD8-7	1.8/1.5	1.8/1.5	1.8	1.8	2.5	—	—
1.5-V LVTTL/LVCMOS	JESD8-11	1.8/1.5	1.8/1.5	1.5	1.5	2.5	—	—
1.2-V LVTTL/LVCMOS	JESD8-12	1.2	1.2	1.2	1.2	2.5	—	—
3.0-V PCI	PCI Rev 2.2	3.0	3.0	3.0	3.0	3.0	—	—
3.0-V PCI-X	PCI-X Rev 1.0	3.0	3.0	3.0	3.0	3.0	—	—
SSTL-2 Class I	JESD8-9B	*(2)*	*(2)*	2.5	2.5	2.5	1.25	1.25
SSTL-2 Class II	JESD8-9B	*(2)*	*(2)*	2.5	2.5	2.5	1.25	1.25
SSTL-18 Class I	JESD8-15	*(2)*	*(2)*	1.8	1.8	2.5	0.90	0.90
SSTL-18 Class II	JESD8-15	*(2)*	*(2)*	1.8	1.8	2.5	0.90	0.90
SSTL-15 Class I	—	*(2)*	*(2)*	1.5	1.5	2.5	0.75	0.75
SSTL-15 Class II	—	*(2)*	*(2)*	1.5	—	2.5	0.75	0.75
HSTL-18 Class I	JESD8-6	*(2)*	*(2)*	1.8	1.8	2.5	0.90	0.90
HSTL-18 Class II	JESD8-6	*(2)*	*(2)*	1.8	1.8	2.5	0.90	0.90
HSTL-15 Class I	JESD8-6	*(2)*	*(2)*	1.5	1.5	2.5	0.75	0.75
HSTL-15 Class II	JESD8-6	*(2)*	*(2)*	1.5	—	2.5	0.75	0.75
HSTL-12 Class I	JESD8-16A	*(2)*	*(2)*	1.2	1.2	2.5	0.6	0.6
HSTL-12 Class II	JESD8-16A	*(2)*	*(2)*	1.2	—	2.5	0.6	0.6

Table 7–2. I/O Standards and Voltage Levels for Stratix III Devices *(Note 1)*, *(3)* (Part 2 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
Differential SSTL-2 Class I	JESD8-9B	*(2)*	*(2)*	2.5	2.5	2.5	—	1.25
Differential SSTL-2 Class II	JESD8-9B	*(2)*	*(2)*	2.5	2.5	2.5	—	1.25
Differential SSTL-18 Class I	JESD8-15	*(2)*	*(2)*	1.8	1.8	2.5	—	0.90
Differential SSTL-18 Class II	JESD8-15	*(2)*	*(2)*	1.8	1.8	2.5	—	0.90
Differential SSTL-15 Class I	—	*(2)*	*(2)*	1.5	1.5	2.5	—	0.75
Differential SSTL-15 Class II	—	*(2)*	*(2)*	1.5	—	2.5	—	0.75
Differential HSTL-18 Class I	JESD8-6	*(2)*	*(2)*	1.8	1.8	2.5	—	0.90
Differential HSTL-18 Class II	JESD8-6	*(2)*	*(2)*	1.8	1.8	2.5	—	0.90
Differential HSTL-15 Class I	JESD8-6	*(2)*	*(2)*	1.5	1.5	2.5	—	0.75
Differential HSTL-15 Class II	JESD8-6	*(2)*	*(2)*	1.5	—	2.5	—	0.75
Differential HSTL-12 Class I	JESD8-16A	*(2)*	*(2)*	1.2	1.2	2.5	—	0.60
Differential HSTL-12 Class II	JESD8-16A	*(2)*	*(2)*	1.2	—	2.5	—	0.60
LVDS *(6)*, *(8)*	ANSI/TIA/EIA-644	*(2)*	*(2)*	2.5	2.5	2.5	—	—
RSDS *(6)*, *(7)*, *(8)*	—	*(2)*	*(2)*	2.5	2.5	2.5	—	—
mini-LVDS *(6)*, *(7)*, *(8)*	—	*(2)*	*(2)*	2.5	2.5	2.5	—	—

Table 7–2. I/O Standards and Voltage Levels for Stratix III Devices *(Note 1)*, *(3)* (Part 3 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
LVPECL	—	*(4)*	*(4)*	—	—	2.5	—	—

Notes to Table 7–2:

(1) V_{CCPD} is either 2.5 V, 3.0 V, or 3.3 V. For V_{CCIO} = 3.3 V, V_{CCPD}=3.3 V. For V_{CCIO} = 3.0 V, V_{CCPD} = 3.0 V. For V_{CCIO} = 2.5 V or less, V_{CCPD} = 2.5 V.

(2) Single-ended HSTL/SSTL, differential SSTL/HSTL, and LVDS input buffers are powered by V_{CCPD}.

(3) $V_{CCCLKIN}$ powers the Column I/O bank dedicated clock input pins when configured as differential inputs. Clock input pins on the Column I/O banks use V_{CCIO} when configured as single-ended inputs.

(4) Column and row I/O banks support LVPECL I/O standards for input operation only on dedicated clock input pins. Clock inputs on column I/O are powered by $V_{CCCLKIN}$ when configured as differential clock input. Differential clock inputs in row I/O are powered by V_{CCPD}.

(5) Row I/O banks support LVDS outputs using a dedicated output buffer. Column and row I/O banks support emulated LVDS outputs using two single-ended output buffers and external one-resistor (LVDS_E_1R) and a three-resistor (LVDS_E_3R) network.

(6) Row I/O banks support RSDS and mini-LVDS I/O standards using a true LVDS output buffer without a resistor network.

(7) Column and row I/O banks support emulated-RSDS and mini-LVDS I/O standards using two single-ended output buffers with one-resistor (RSDS_E_1R and mini-LVDS_E_1R) and three-resistor (RSDS_E_3R and mini-LVDS_E_3R) networks.

(8) The emulated differential output standard that supports the tri-state feature includes: LVDS_E_1R, LVDS_E_3R, RSDS_E_1R, RSDS_E_3R, Mini_LVDS_E_1R, and Mini_LVDS_E_3R.

For detailed electrical characteristics of each I/O standard, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter.

Stratix III I/O Banks

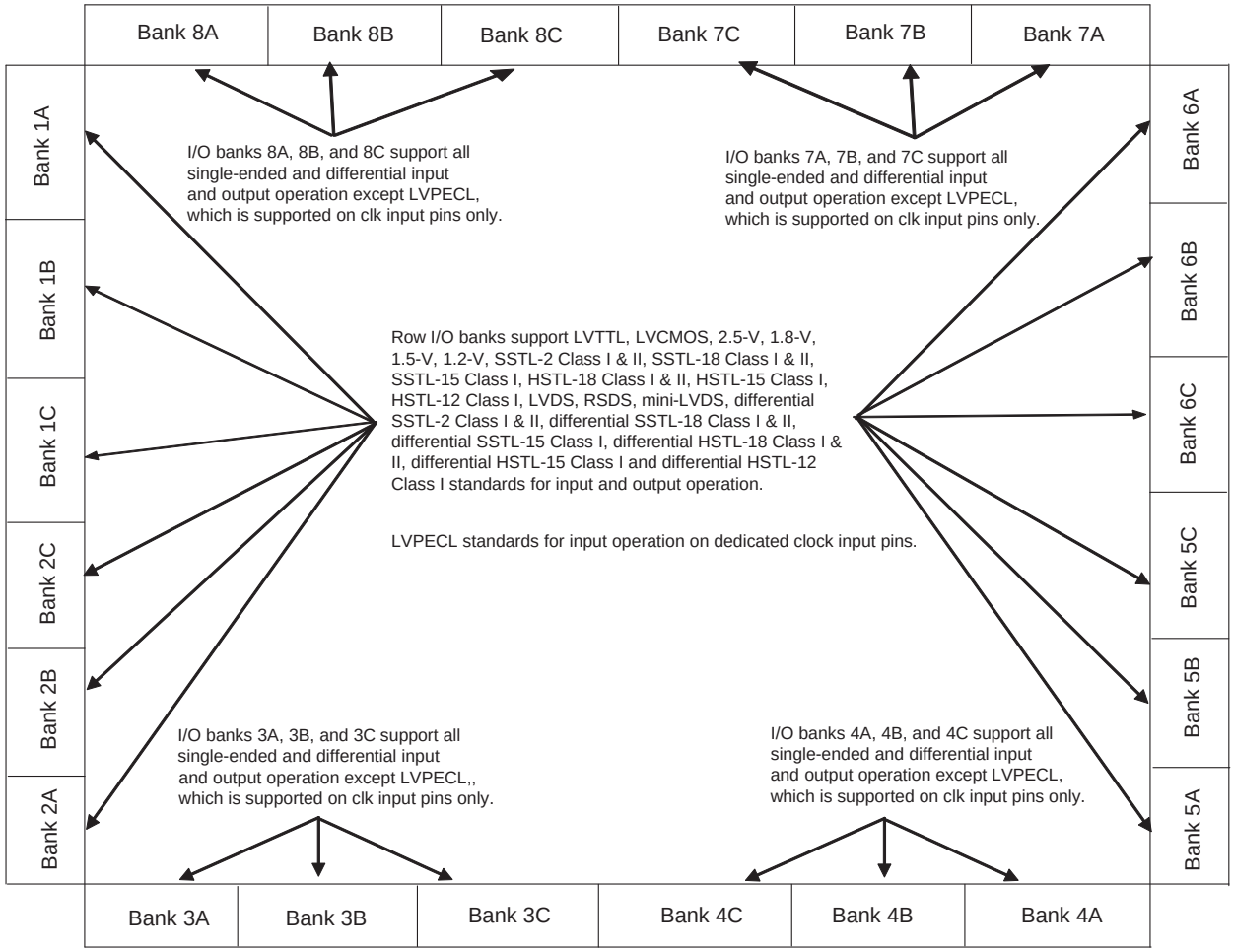
Stratix III devices contain up to 24 I/O banks, as shown in Figure 7–1. The row I/O banks contain true differential input and output buffers and dedicated circuitry to support differential standards at speeds up to 1.6 Gbps.

Every I/O bank in Stratix III devices can support high-performance external memory interfaces with dedicated circuitry. The I/O pins are organized in pairs to support differential standards. Each I/O pin pair can support both differential input and output buffers. The only exceptions are the `CLK[1,3,8,10][p,n]`, `PLL_L[1,4]_CLK[p,n]`, and `PLL_R[1,4]_CLK[p,n]` pins, which support differential or single-ended input operations, these pins do not support output operations.

Pins that do not support output operations do not support the programmable current strength, programmable slew rate, programmable pull-up, bus hold, open-drain, or on-chip series termination (OCT R_S) options.

For the number of channels available for the LVDS I/O standard, refer to the *High-Speed Differential I/O Interface with DPA in Stratix III Devices* chapter.

Figure 7–1. I/O Banks for Stratix III Devices *(Note 1)*, *(2)*, *(3)*, *(4)*, *(5)*, *(6)*, *(7)*, *(8)*, *(9)*


Bank 8A
Bank 8B
Bank 8C
Bank 7C
Bank 7B
Bank 7A
Bank 1A
Bank 1B
Bank 1C
Bank 2C
Bank 2B
Bank 2A
Bank 6A
Bank 6B
Bank 6C
Bank 5C
Bank 5B
Bank 5A
Bank 3A
Bank 3B
Bank 3C
Bank 4C
Bank 4B
Bank 4A
I/O banks 8A, 8B, and 8C support all single-ended and differential input and output operation except LVPECL, which is supported on clk input pins only.
I/O banks 7A, 7B, and 7C support all single-ended and differential input and output operation except LVPECL, which is supported on clk input pins only.
Row I/O banks support LVTTL, LVCMOS, 2.5-V, 1.8-V, 1.5-V, 1.2-V, SSTL-2 Class I & II, SSTL-18 Class I & II, SSTL-15 Class I, HSTL-18 Class I & II, HSTL-15 Class I, HSTL-12 Class I, LVDS, RSDS, mini-LVDS, differential SSTL-2 Class I & II, differential SSTL-18 Class I & II, differential SSTL-15 Class I, differential HSTL-18 Class I & II, differential HSTL-15 Class I and differential HSTL-12 Class I standards for input and output operation.
LVPECL standards for input operation on dedicated clock input pins.
I/O banks 3A, 3B, and 3C support all single-ended and differential input and output operation except LVPECL,, which is supported on clk input pins only.
I/O banks 4A, 4B, and 4C support all single-ended and differential input and output operation except LVPECL, which is supported on clk input pins only.

Notes to Figure 7–1:

(1) Differential HSTL and SSTL outputs are not true differential outputs. They use two single-ended outputs with the second output programmed as inverted.

(2) Column and row I/O differential HSTL and SSTL inputs use LVDS differential input buffers without OCT R_D support.

(3) Column and row I/O supports emulated LVDS output buffer.

(4) Column I/O supports PCI/PCI-X with on-chip clamp diode, and row I/O supports PCI/PCI-X with external clamp diode.

(5) Clock inputs on column I/O are powered by $V_{CCCLKIN}$ when configured as differential clock input. They are powered by V_{CCIO} when configured as single-ended clock input. All outputs use the corresponding bank V_{CCIO}.

(6) Row I/O supports the true LVDS output buffer.

(7) Column and row I/O banks support LVPECL standards for input operation on dedicated clock input pins.

(8) Figure 7–1 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(9) 3.0-V PCI/PCI-X and 3.3-V LVTTL/LVCMOS outputs are not supported in the same I/O bank.

Modular I/O Banks

The I/O pins in Stratix III devices are arranged in groups called modular I/O banks. Depending on device densities, the number of I/O banks range from 16 to 24 banks. The size of each bank is 24, 32, 36, 40, or 48 I/O pins. Figure 7–3 to Figure 7–5 show the number of I/O pins available in each I/O bank and packaging information for different sets of available devices.

In Stratix III devices, the maximum number of I/O banks per side is four or six, depending on the device density. When migrating between devices with a different number of I/O banks per side, it is the middle or "B" bank which is removed or inserted. For example, when moving from a 24-bank device to a 16-bank device, the banks that are dropped are "B" banks, namely: 1B, 2B, 3B, 4B, 5B, 6B, 7B, and 8B. Similarly, when moving from a 16-bank device to a 24-bank device, the banks that are added are "B" banks, namely: 1B, 2B, 3B, 4B, 5B, 6B, 7B, and 8B.

During migration from a smaller device to a larger device, the bank size increases or remains the same but never decreases. For example, banks may increase from a size of 24 I/O to a bank of size 32, 36, 40, or 48 I/O, but never decrease. Table 7–3 lists the increase in bank size when migrating from a smaller device to a larger device.

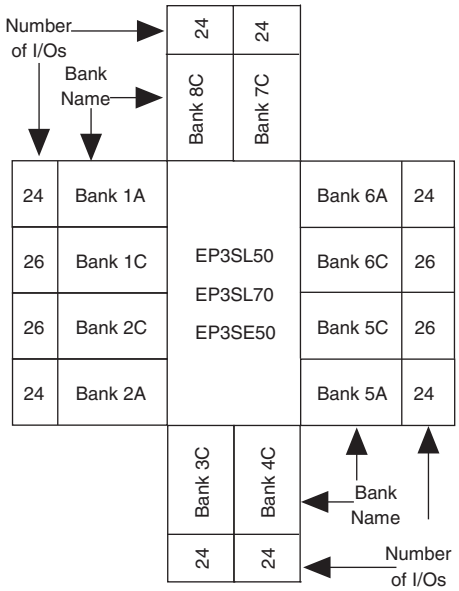
Table 7–3. Bank Migration Path with Increasing Device Size *(Note 1)*

	Banks	Increase in Bank Size (number of I/O)		
Column I/O	A	40	48	—
	B	24	48	—
	C	24	32	48
Row I/O	A	32	48	—
	B	24	36	—
	C	24	40	48

Note to Table 7–3:

(1) Number of I/O shown does not include dedicated clock input pins `CLK[1,3,8,10][p,n]`.

Figure 7–2. Number of I/Os in Each Bank in EP3SL50, EP3SL70, and EP3SE50 Devices in 484-Pin FineLine BGA Package *(Note 1)*, *(2)*,

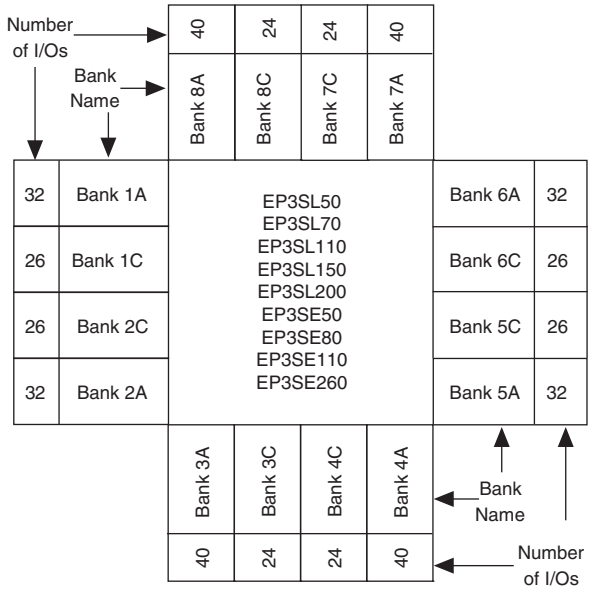


Notes to Figure 7–2:

(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the pin count.

(2) Figure 7–2 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Figure 7–3. Number of I/Os in Each Bank in the 780-pin FineLine BGA Package *(Note 1)*, *(2)*, *(3)*, *(4)*



Notes to Figure 7–3:

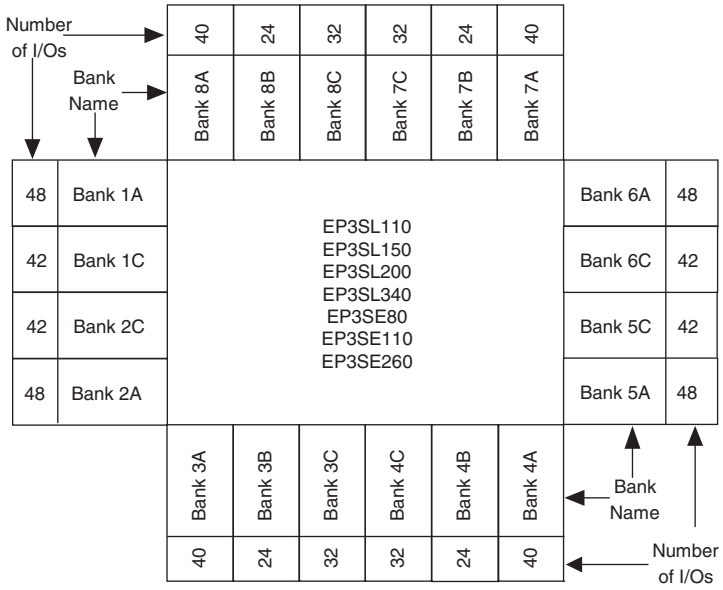
(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(2) Figure 7–3 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(3) Number of I/Os in each Bank in EP3SL50,EP3SL70, EP3SL110, EP3SL150, EP3SE50, EP3SE80 and EP3SE110 in the 780-pin FineLine BGA package.

(4) Number of I/Os in each Bank in EP3SL200 and EP3SE260 in the 780-pin Hybrid FineLine BGA package.

Figure 7–4. Number of I/Os in Each Bank in the 1152-pin FineLine BGA Package *(Note 1)*, *(2)*, *(3)*, *(4)*



Notes to Figure 7–4:

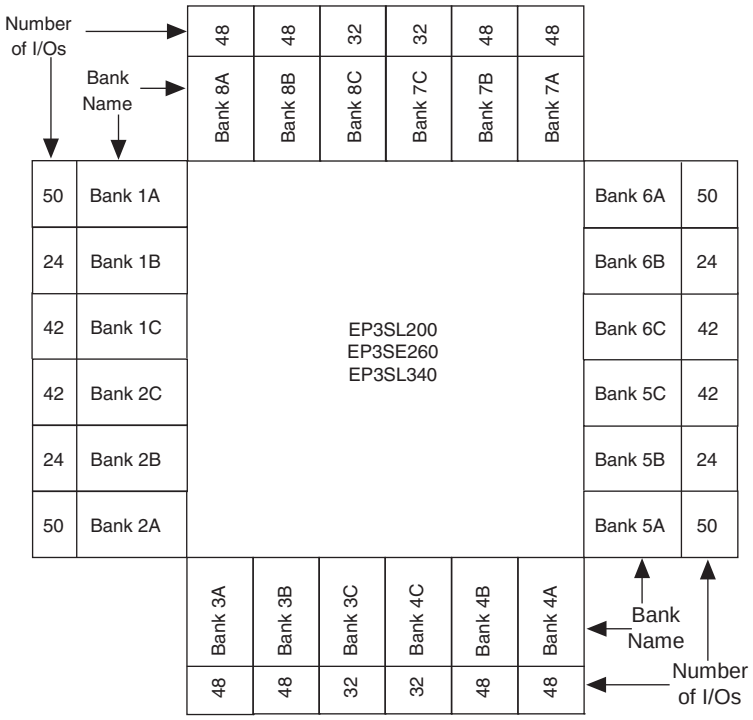
(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(2) Figure 7–4 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(3) Number of I/Os in Each Bank in EP3SL110, EP3SL150, EP3SL200, EP3SE80, EP3SE110, and EP3SE260 Devices in the 1152-pin FineLine BGA package.

(4) Number of I/Os in Each Bank in EP3SL340 in the 1152-pin Hybrid FineLine BGA package.

Figure 7–5. Number of I/Os in Each Bank in EP2SL200, EP3SE260, and EP3SL340 Devices in the 1517-Pin FineLine BGA Package *(Note 1)*, *(2)*

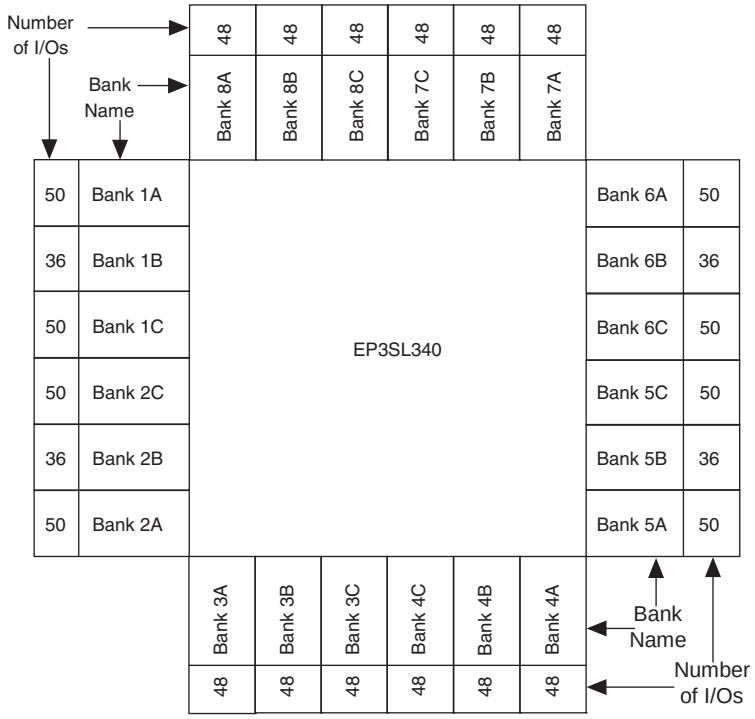


Notes to Figure 7–5:

(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(2) Figure 7–5 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Figure 7–6. Number of I/Os in Each Bank in EP3SL340 Devices in the 1760-pin FineLine BGA Package *(Note 1)*, *(2)*



Notes to Figure 7–6:

(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(2) Figure 7–6 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Stratix III I/O Structure

The I/O element (IOE) in Stratix III devices contains a bi-directional I/O buffer and I/O registers to support a complete embedded bi-directional single data rate or DDR transfer. The IOEs are located in I/O blocks around the periphery of the Stratix III device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row IOEs drive row, column, or direct link interconnects. The column IOEs drive column interconnects.

The Stratix III bi-directional IOE also supports the following features:

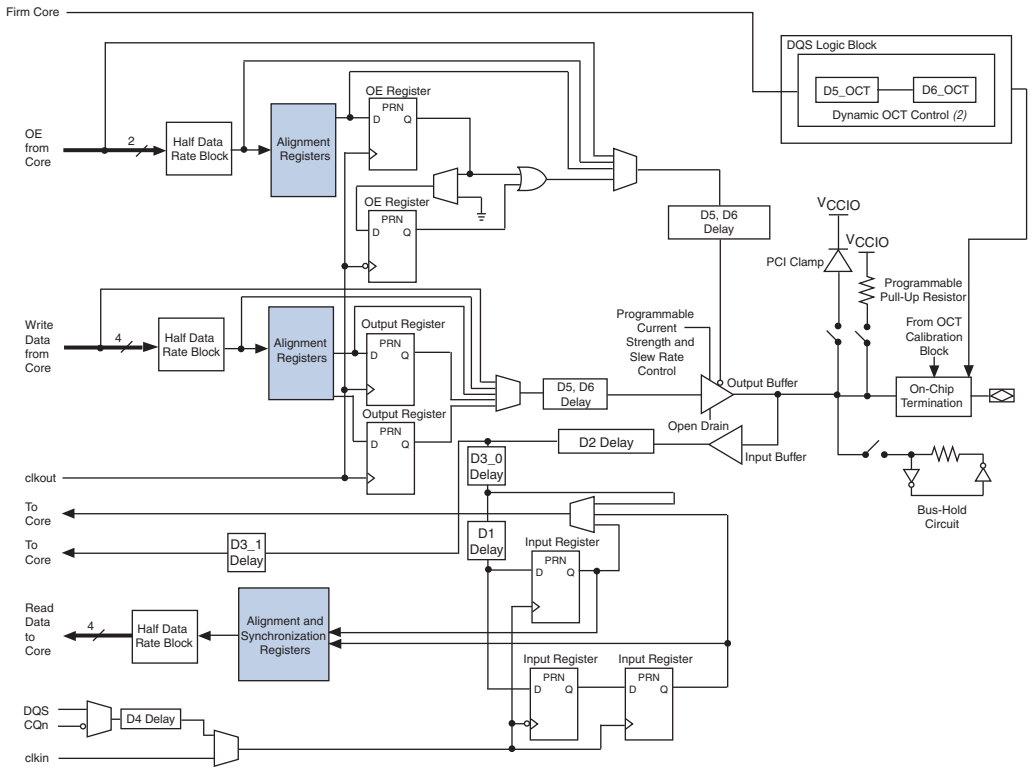
- Programmable input delay
- Programmable output-current strength
- Programmable slew rate
- Programmable output delay
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- On-chip series termination with calibration

- On-chip series termination without calibration
- On-chip parallel termination with calibration (OCT R_T)
- On-chip differential termination (OCT R_D)
- PCI clamping diode

The I/O registers are composed of the input path for handling data from the pin to the core, the output path for handling data from the core to the pin, and the output-enable (OE) path for handling the OE signal for the output buffer. These registers allow faster source-synchronous register-to-register transfers and resynchronization. The input path consists of the DDR input registers, alignment and synchronization registers, and HDR. You can bypass each block of the input path.

Figure 7–7 shows the Stratix III IOE structure.

Figure 7–7. IOE Structure for Stratix III Devices *(Note 1)*, *(2)*



Notes to Figure 7–7:

(1) D3_0 and D3_1 delays have the same available settings in the Quartus® II software.

(2) One dynamic OCT control is available per DQ/DQS group.

The output and OE paths are divided into output or OE registers, alignment registers, and HDR blocks. You can bypass each block of the output and OE path.

For more information about I/O registers and how they are used for memory applications, refer to the *External Memory Interfaces in Stratix III Devices* chapter.

3.3-V I/O Interface

Stratix III I/O buffers are fully compatible with 3.3-V I/O standards, and you can use them as transmitters or receivers in your system. The output high voltage (V_{OH}), output low voltage (V_{OL}), input high voltage (V_{IH}), and input low voltage (V_{IL}) levels meet the 3.3-V I/O standards specifications defined by EIA/JEDEC Standard JESD8-B with margin when the Stratix III V_{CCIO} voltage is powered by 3.3 V or 3.0 V.

For device reliability and proper operation when interfacing with a 3.3 V I/O system using Stratix III devices, ensure that the absolute maximum ratings of Stratix III devices are not violated. Altera recommends performing IBIS simulation to determine that the overshoot and undershoot voltages are within the guidelines.

When using a Stratix III device as a transmitter, some techniques can limit the overshoot and undershoot at the I/O pins, such as slow slew rate and series termination, but they are not mandatory. Transmission line effects that cause large voltage deviation at the receiver are associated with impedance mismatch between the driver and transmission line. By matching the impedance of the driver to the characteristic impedance of the transmission line, overshoot voltage can be significantly reduced. You can use a series termination resistor placed physically close to the driver to match the total driver impedance to the transmission line impedance. Stratix III devices support OCT R_S for all LVTTL/LVCMOS I/O standards in all I/O banks.

When using a Stratix III device as a receiver, a clamping diode can be used to limit the overshoot (on-chip or off-chip), but it is not mandatory. Stratix III devices provide an optional on-chip PCI-clamp diode for column I/O pins. You can use this diode to protect I/O pins against overshoot voltage.

Another method for limiting overshoot is reducing the bank supply voltage (V_{CCIO}) to 3.0 V. With this method, the clamp diode (on-chip or off-chip), though not mandatory, can sufficiently clamp overshoot voltage to within the DC and AC input voltage specification. The clamped voltage can be expressed as the sum of the supply voltage (V_{CCIO}) and the diode forward voltage. By lowering V_{CCIO} to 3.0 V you can reduce overshoot and undershoot for all I/O standards, including 3.3-V LVTTL/LVCMOS, 3.0-V LVTTL/LVCMOS, and 3.0-V PCI/PCI-X. Additionally, lowering V_{CCIO} to 3.0 V reduces power consumption.

For more information about absolute maximum rating and maximum allowed overshoot during transitions, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter.

External Memory Interfaces

In addition to the I/O registers in each IOE, Stratix III devices also have dedicated registers and phase-shift circuitry on all I/O banks for interfacing with external memory interfaces. Table 7–4 lists the memory interfaces and the corresponding I/O standards supported by Stratix III devices.

Table 7–4. Memory Interface Standards Supported (Part 1 of 2)

Memory Interface Standard	I/O Standard
DDR SDRAM	SSTL-2
DDR2 SDRAM	SSTL-18

Table 7–4. Memory Interface Standards Supported (Part 2 of 2)

Memory Interface Standard	I/O Standard
DDR3 SDRAM	SSTL-15
RLDRAM II	HSTL-18
QDR II SRAM	HSTL-18
QDR II+ SRAM	HSTL-15

For more information about external memory interfaces, refer to the *External Memory Interfaces in Stratix III Devices* chapter.

High-Speed Differential I/O with DPA Support

Stratix III devices contain dedicated circuitry for supporting differential standards at speeds up to 1.6 Gbps. The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications: Utopia IV, SPI-4.2, SFI-4, 10 Gigabit Ethernet XSBI, RapidIOTM, and NPSI. Stratix III devices support ×2, ×4, ×6, ×7, ×8, and ×10 SERDES modes for high-speed differential I/O interfaces and ×4, ×6, ×7, ×8, and ×10 SERDES modes with dedicated DPA circuitry. DPA minimizes bit errors, simplifies PCB layout and timing management for high-speed data transfer, and eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.

×2 mode is supported by the DDR registers and is not included in SERDES. For Stratix III devices, SERDES can be bypassed in the Quartus II MegaWizard™ Plug-In Manager for the ALTLVDS megafunction to support DDR (×2) operation.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- DPA
- Synchronizer (FIFO buffer)
- Phase-locked loops (PLLs)

For more information about DPA support, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter.

Programmable Current Strength

The output buffer for each Stratix III device I/O pin has a programmable current-strength control for certain I/O standards. You can use programmable current strength to mitigate the effects of high signal attenuation due to a long transmission line or a legacy backplane. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of current strength that you can control. Table 7–5 lists information about programmable current strength.

Table 7–5. Programmable Current Strength *(Note 1)*

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	16, 12, 8, 4	8, 4
3.0-V LVTTL	16, 12, 8, 4	12, 8, 4
3.0-V LVCMOS	16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.2-V LVTTL/LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 10, 8	12, 8
SSTL-2 Class II	16	16
SSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
SSTL-18 Class II	16, 8	16, 8
SSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
SSTL-15 Class II	16, 8	—
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
HSTL-18 Class II	16	16
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	16	—
HSTL-12 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-12 Class II	16	—

Note to Table 7–5:

(1) The default setting in the Quartus II software is 50-Ω OCT R_S without calibration for all non-voltage reference and HSTL/SSTL class I I/O standards. The default setting is 25-Ω OCT R_S without calibration for HSTL/SSTL class II I/O standards.

Altera recommends performing IBIS or SPICE simulations to determine the right current strength setting for your specific application.

Programmable Slew Rate Control

The output buffer for each Stratix III device regular- and dual-function I/O pin has a programmable output slew-rate control that you can configure for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. A slow slew rate can help reduce system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis.

You cannot use the programmable slew rate feature when using OCT R_S.

The Quartus II software allows four settings for programmable slew rate control—0, 1, 2, and 3—where 0 is slow slew rate and 3 is fast slew rate. Table 7–6 lists the default setting for the I/O standards supported in the Quartus II software.

Table 7–6. Default Programmable Slew Rate

I/O Standard	Default Slew Rate Setting
1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.0-V, and 3.3-V LVTTL / LVCMOS	3
3.0-V PCI / PCI-X	3
SSTL-2, -18, -15 Class I and Class II	3
HSTL-18, -15, -12 Class I and II	3
Differential SSTL-2, -18, -15 Class I and Class II	3
Differential HSTL-18, -15, -12 Class I and Class II	3
LVDS_E_1R, mini-LVDS_E_1R, RSDS_E_1R	3
LVDS_E_3R, mini-LVDS_E_3R, RSDS_E_3R	3

You can use faster slew rates to improve the available timing margin in memory-interface applications or when the output pin has high-capacitive loading. Altera recommends performing IBIS or SPICE simulations to determine the right slew rate setting for your specific application.

Programmable Delay

The Stratix III device IOE includes programmable delays (refer to Figure 7–7) that you can activate to ensure zero hold times, minimize setup times, or increase clock-to-output times. Each pin can have a different input delay from pin to input register or a delay from the output register to the output pin values to ensure that the bus has the same delay going into or out of the device. This feature helps read and time margins as it minimizes the uncertainties between signals in the bus.

For the programmable IOE delay specifications, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter.

Programmable Output Buffer Delay

Stratix III devices support delay chains built inside the single-ended output buffer, as shown in Figure 7–7 on page 7–13. The delay chains can independently control the rising and falling edge delays of the output buffer, providing the ability to adjust the output-buffer duty cycle, compensate channel-to-channel skew, reduce simultaneous switching output (SSO) noise by deliberately introducing channel-to-channel skew, and improve high-speed memory-interface timing margins. Stratix III devices support four levels of output buffer delay settings. The default setting is **No Delay**.

For the programmable output buffer delay specifications, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter.

Open-Drain Output

Stratix III devices provide an optional open-drain output (equivalent to an open-collector output) for each I/O pin. When configured as open-drain, the logic value of the output is either `high-Z` or `0`. Typically, an external pull-up resistor is required to provide logic high.

Bus Hold

Each Stratix III device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, you do not need an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls non-driven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent over-driving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature if the I/O pin is configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to weakly pull the signal level to the last-driven state.

For the specific sustaining current driven through this resistor and the overdrive current used to identify the next-driven input level, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix III device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the I/O to the V_{CCIO} level.

Programmable pull-up resistors are only supported on user I/O pins and are not supported on dedicated configuration pins, JTAG pins, or dedicated clock pins. If the programmable pull-up option is enabled, you cannot use the bus-hold feature.

When the optional `DEV_OE` signal drives low, all I/O pins remain tri-stated even with programmable pull-up option enabled.

Programmable Pre-Emphasis

Stratix III LVDS transmitters support programmable pre-emphasis to compensate for the frequency dependent attenuation of the transmission line. The Quartus II software allows four settings for programmable pre-emphasis—zero, low, medium, and high. The default setting is low.

For more information about programmable pre-emphasis, refer to the *High-Speed Differential I/O Interfaces with DPA* in the *Stratix III Devices* chapter.

Programmable Differential Output Voltage

Stratix III LVDS transmitters support programmable V_{OD}. The programmable V_{OD} settings enable you to adjust output eye height to optimize for trace length and power consumption. A higher V_{OD} swing improves voltage margins at the receiver end while a smaller V_{OD} swing reduces power consumption. The Quartus II software allows four settings for programmable V_{OD}—low, medium low, medium high, and high. The default setting is medium low.

For more information about programmable V_{OD}, refer to the *High Speed Differential I/O Interfaces with DPA in the Stratix III Devices* chapter.

MultiVolt I/O Interface

The Stratix III architecture supports the MultiVolt™ I/O interface feature that allows Stratix III devices in all packages to interface with systems of different supply voltages.

You can connect the V_{CCIO} pins to a 1.2-, 1.5-, 1.8-, 2.5-, 3.0 or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply. (For example, when V_{CCIO} pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems.)

You must connect the Stratix III VCCPD power pins to a 2.5-, 3.0 or 3.3-V power supply. Using these power pins to supply the pre-driver power to the output buffers increases the performance of the output pins. Table 7–7 summarizes Stratix III MultiVolt I/O support.

For V_{CCIO} = 3.3 V, V_{CCPD}=3.3 V. For V_{CCIO} = 3.0 V, V_{CCPD} = 3.0 V. For V_{CCIO} = 2.5 V or less, V_{CCPD} = 2.5 V.

Table 7–7. MultiVolt I/O Support for Stratix III Devices *(Note 1)*, *(2)*

V_{CCIO} (V)	Input Signal (V)						Output Signal (V)					
	1.2	1.5	1.8	2.5	3.0	3.3	1.2	1.5	1.8	2.5	3.0	3.3
1.2	✓	—	—	—	—	—	✓	—	—	—	—	—
1.5	—	✓	✓ *(1)*	—	—	—	—	✓	—	—	—	—
1.8	—	✓	✓	—	—	—	—	—	✓	—	—	—
2.5	—	—	—	✓	✓ *(2)*	✓ *(2)*	—	—	—	✓	—	—
3.0	—	—	—	✓	✓	✓	—	—	—	—	✓	—
3.3	—	—	—	✓	✓	✓	—	—	—	—	—	✓

Notes to Table 7–7:

(1) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Stratix III V_{IL} maximum and V_{IH} minimum voltage specifications.

(2) Use on-chip PCI clamp diode for column I/Os or external PCI clamp diode for row I/Os to protect the input pins against overshoot voltage.

(3) Each I/O bank of a Stratix III device has its own VCCIO pins and supports only one V_{ccio}, either 1.2, 1.5, 1.8, or 3.0 V. The LVDS I/O standard requires that a V_{CCIO} of 2.5 V cannot be assigned in a same bank with a 3.0-V or 3.3-V output signal.

OCT Support

Stratix III devices feature dynamic series and parallel on-chip termination to provide I/O impedance matching and termination capabilities. OCT improves signal quality over external termination by reducing parasitic, saving board space, and reducing external component costs.

Stratix III devices support OCT R_S with or without calibration, OCT R_T with calibration, and dynamic series and parallel termination for single-ended I/O standards as well as OCT R_D for differential LVDS I/O standards. Stratix III devices support OCT in all I/O banks by selecting one of the OCT I/O standards.

Stratix III devices support OCT R_S and R_T in the same I/O bank for different I/O standards if they use the same V_{CCIO} supply voltage. Each I/O in an I/O bank can be independently configured to support OCT R_S, programmable current strength, or OCT R_T.

☞ You cannot configure both OCT R_S and programmable current strength for the same I/O buffer.

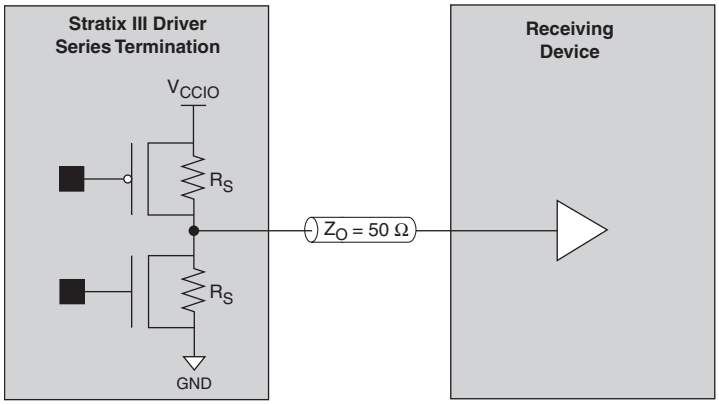
A pair of RUP and RDN pins are available in a given I/O bank, and are shared for series- and parallel-calibrated termination. The RUP and RDN pins share the same V_{CCIO} and GND, respectively, with the I/O bank where they are located. The RUP and RDN pins are dual-purpose I/Os, and function as regular I/Os if you do not use the calibration circuit. When used for calibration, the RUP pin is connected to V_{CCIO} through an external 25-Ω ±1% or 50-Ω ±1% resistor for an OCT R_S value of 25 Ω or 50 Ω, respectively; the RDN pin is connected to GND through an external 25-Ω ±1% or 50-Ω ±1% resistor for an OCT R_S value of 25 Ω or 50 Ω, respectively. For OCT R_T, the RUP pin is connected to V_{CCIO} through an external 50-Ω ±1% resistor; the RDN pin is connected to GND through an external 50-Ω ±1% resistor.

On-Chip Series Termination without Calibration

Stratix III devices support driver-impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, you can significantly reduce reflections. Stratix III devices support OCT R_S for single-ended I/O standards (see Figure 7–8).

The R_S shown in Figure 7–8 is the intrinsic impedance of the output transistors. The typical R_S values are 25 Ω and 50 Ω. When matching impedance is selected, current strength is no longer selectable.

Figure 7–8. On-Chip Series Termination without Calibration for Stratix III Devices



To use OCT for the SSTL Class I standard, you should select the **50-Ω on-chip series termination** setting, eliminating the external 25-Ω R_S (to match the 50-Ω transmission line). For the SSTL Class II standard, you should select the **25-Ω on-chip series termination** setting (to match the 50-Ω transmission line and the near-end external 50-Ω pull-up to V_{TT}).

On-Chip Series Termination with Calibration

Stratix III devices support OCT R_S with calibration in all banks. The OCT R_S calibration circuit compares the total impedance of the I/O buffer to the external 25-Ω ±1% or 50-Ω ±1% resistors connected to the RUP and RDN pins, and dynamically enables or disables the transistors until they match. The R_S shown in Figure 7–9 is the intrinsic impedance of transistors. Calibration occurs at the end of device configuration. When the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers. When calibration is not taking place, the RUP and RDN pins go to a tri-state condition.

Figure 7–9. On-Chip Series Termination with Calibration for Stratix III Devices

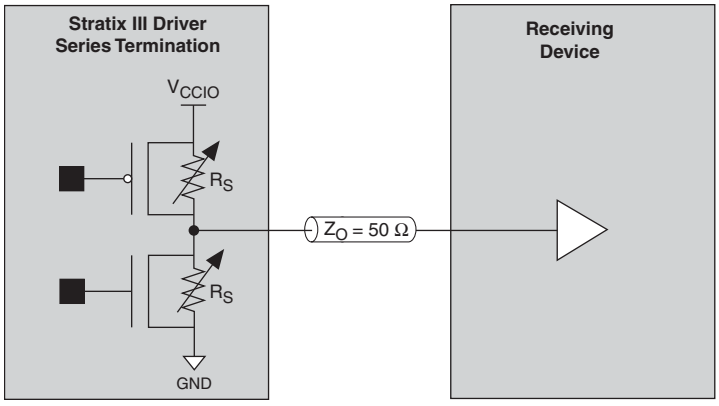


Table 7–8 lists I/O standards that support OCT R_S with calibration.

Table 7–8. Selectable I/O Standards with On-Chip Series Termination With or Without Calibration

I/O Standard	On-Chip Series Termination Setting		
	Row I/O	Column I/O	Unit
3.3-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
3.0-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
2.5-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
1.8-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
1.5-V LVTTL/LVCMOS	50	50	Ω
		25	Ω
1.2-V LVTTL/LVCMOS	50	50	Ω
		25	Ω
SSTL-2 Class I	50	50	Ω
SSTL-2 Class II	25	25	Ω
SSTL-18 Class I	50	50	Ω
SSTL-18 Class II	25	25	Ω
SSTL-15 Class I	50	50	Ω
SSTL-15 Class II	—	25	Ω
HSTL-18 Class I	50	50	Ω
HSTL-18 Class II	25	25	Ω
HSTL-15 Class I	50	50	Ω
HSTL-15 Class II	—	25	Ω
HSTL-12 Class I	50	50	Ω
HSTL-12 Class II	—	25	Ω

Expanded On-Chip Series Termination with Calibration

OCT calibration circuits always adjust OCT R_S to match the external resistors connected to the RUP and RDN pins, it is possible to achieve different OCT R_S values besides the 25- and 50-Ω resistors. Theoretically you can always change the resistance connected to the RUP and RDN pins accordingly if you require a different OCT R_S value. Practically, the OCT R_S range, which Stratix III devices can support, is limited due to the output buffer size and granularity limitations. Table 7–9 shows expanded OCT R_S with calibration supported in Stratix III devices.The Quartus II software only allows discrete OCT R_S calibration settings of 25 Ω, 40 Ω, 50 Ω, and 60 Ω. You can select the closest discrete value of OCT R_S with calibration settings in the Quartus II software to your system to get the closest timing and IBIS model information. For example, if you use 20-Ω OCT R_S with calibration in your system, you can select 25-Ω OCT R_S with calibration setting in the Quartus II software to get the closest timing and IBIS model information.

Table 7–9. Selectable I/O Standards with Expanded On-Chip Series Termination with Calibration Range

I/O Standard	Expanded OCT R_s range		
	Row I/O	Column I/O	Unit
3.3-V LVTTL/LVCMOS	20–60	20–60	Ω
3.0-V LVTTL/LVCMOS	20–60	20–60	Ω
2.5-V LVTTL/LVCMOS	20–60	20–60	Ω
1.8-V LVTTL/LVCMOS	20–60	20–60	Ω
1.5-V LVTTL/LVCMOS	40–60	20–60	Ω
1.2-V LVTTL/LVCMOS	40–60	20–60	Ω
SSTL-2	20–60	20–60	Ω
SSTL-18	20–60	20–60	Ω
SSTL-15	40–60	20–60	Ω
HSTL-18	20–60	20–60	Ω
HSTL-15	40–60	20–60	Ω
HSTL-12	40–60	20–60	Ω

Note to Table 7–9:

(1) The expanded On-Chip Series Termination with calibration of SSTL and HSTL is for impedance matching to improve signal integrity and not for meeting JEDEC standard.

Left Shift Series Termination Control

Stratix III devices support left shift series termination control. You can use the left shift series termination control to get the calibrated OCT R_S with half of the impedance value of the external reference resistors connected to RUP and RDN pins. This feature is useful in applications which require both 25-Ω and 50-Ω calibrated OCT R_S at the same V_{CCIO}. For example, if your applications require 25-Ω and 50-Ω calibrated OCT R_S for SSTL–2 Class I and Class II I/O standards, you would only require one OCT calibration block with 50-Ω external reference resistors. You can enable this feature in the ALTIOBUF megafunction in the Quartus II software. The Quartus II software only allows the left shift series termination control for 25-Ω calibrated OCT R_S with 50-Ω external reference resistors connected to RUP and RDN pins. You can only use left shift series termination control for I/O standards that support 25 Ω-calibrated OCT R_S .

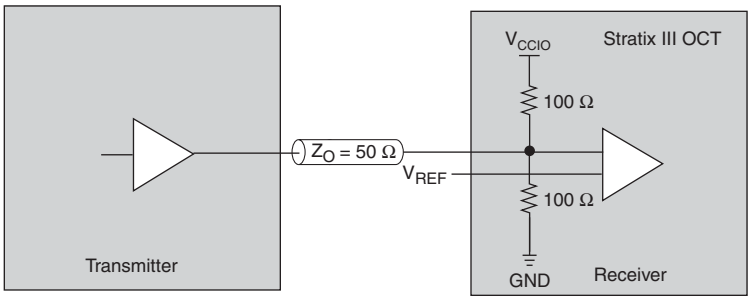
Left shift series termination control is automatically enabled if you use a bidirectional I/O with 25- Ω calibrated OCT R_S and 50- Ω parallel OCT.

For more information about how to enable left shift series termination in the ALTIOBUF megafunction, refer to the *ALTIOBUF Megafunction User Guide*.

On-Chip Parallel Termination with Calibration

Stratix III devices support OCT R_T with calibration in all banks. OCT R_T with calibration is only supported for input or bi-directional pin configurations. For input pins, you can enable OCT R_T continuously. However, for bi-directional I/O, OCT R_T is enabled or disabled depending on whether or not the bi-directional I/O acts as a transmitter or receiver. Output pin configurations do not support OCT R_T with calibration. Figure 7–10 shows OCT R_T with calibration. When OCT R_T is used, the V_{CCIO} of the bank has to match the I/O standard of the pin where the parallel OCT is enabled.

Figure 7–10. On-Chip Parallel Termination with Calibration for Stratix III Devices



The OCT R_T calibration circuit compares the total impedance of the I/O buffer to the external 50-Ω ±1% resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. When the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers. Table 7–10 lists the I/O standards that support OCT R_T with calibration.

Table 7–10. Selectable I/O Standards that Support On-Chip Parallel Termination with Calibration

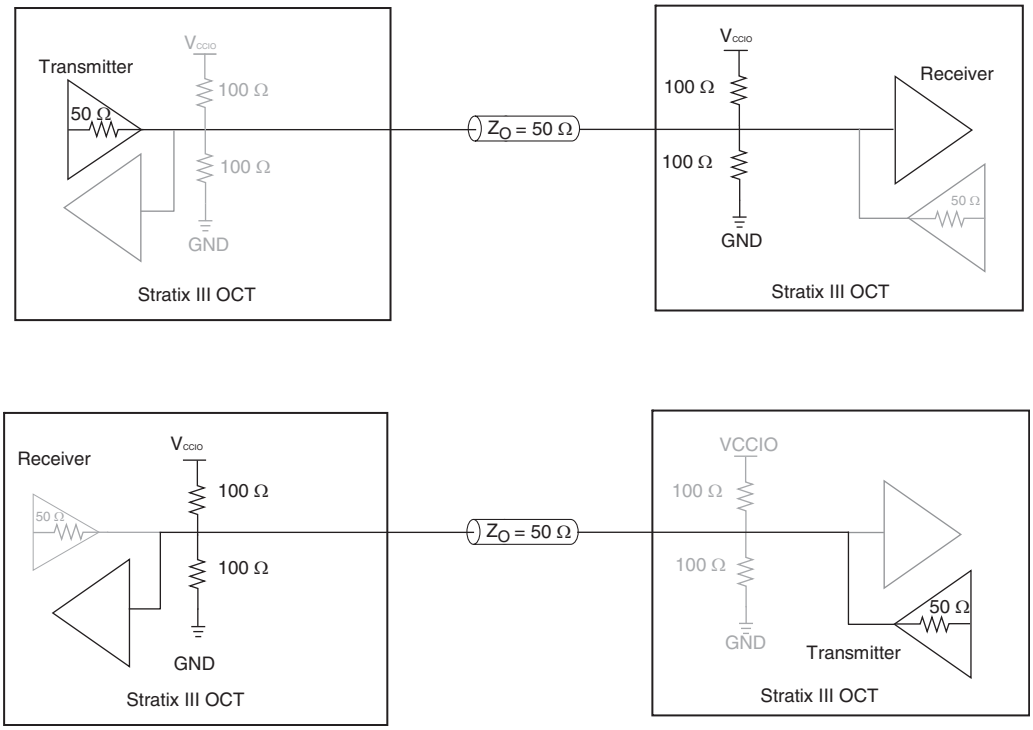
I/O Standard	On-Chip Parallel Termination Setting (Column I/O)	On-Chip Parallel Termination Setting (Row I/O)	Unit
SSTL-2 Class I, II	50	50	Ω
SSTL-18 Class I, II	50	50	Ω
SSTL-15 Class I, II	50	50	Ω
HSTL-18 Class I, II	50	50	Ω
HSTL-15 Class I, II	50	50	Ω
HSTL-12 Class I, II	50	50	Ω
Differential SSTL-2 Class I, II	50	50	Ω
Differential SSTL-18 Class I, II	50	50	Ω
Differential SSTL-15 Class I, II	50	50	Ω
Differential HSTL-18 Class I, II	50	50	Ω
Differential HSTL-15 Class I, II	50	50	Ω
Differential HSTL-12 Class I, II	50	50	Ω

Dynamic OCT

Stratix III devices support on-off dynamic series and parallel termination for a bi-directional I/O in all I/O banks. Figure 7–11 shows the termination schemes supported in the Stratix III device. Dynamic parallel termination is enabled only when the bi-directional I/O acts as a receiver and is disabled when it acts as a driver. Similarly, dynamic series termination is enabled only when the bi-directional I/O acts as a driver and is disabled when it acts as a receiver. This feature is useful for terminating any high-performance bi-directional path because the signal integrity is optimized depending on the direction of the data.

You should connect a bi-directional pin that uses both 25-Ω or 50-Ω series termination and 50-Ω input termination to a calibration block that has a 50-Ω external resistor connected to its RUP and RDN pins. The 25-Ω series termination on the bi-directional pin is achieved through internal divide by two circuits.

Figure 7–11. Dynamic Parallel OCT in Stratix III Devices

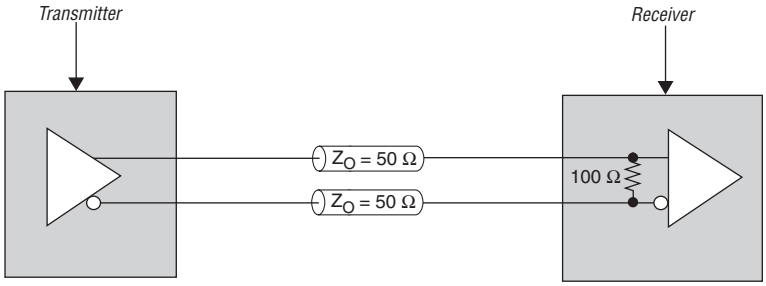


For more information about tolerance specifications for OCT with calibration, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter.

LVDS Input On-Chip Termination (R_D)

Stratix III devices support OCT for differential LVDS input buffers with a nominal resistance value of 10 Ω, as shown in Figure 7–12. You can enable OCT R_D in row I/O banks when V_{CCIO} and V_{CCPD} are set to 2.5 V. The column I/O banks do not support OCT R_D. The dedicated clock input pairs `CLK[1,3,8,10][p,n]`, `PLL_L[1,4]_CLK[p,n]`, and `PLL_R[1,4]_CLK[p,n]` on the row I/O banks of the Stratix III devices do not support OCT R_D. Dedicated clock input pairs `CLK[0,2,9,11][p,n]` on row I/O banks support OCT R_D. Dedicated clock input pairs `CLK[4,5,6,7][p,n]` and `CLK[12,13,14,15][p,n]` on column I/O banks do not support OCT R_D.

Figure 7–12. Differential Input On-Chip Termination



For more information about OCT R_D, refer to the *High Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter.

Table 7–11 lists the assignment name and its value for OCT R_D in the Quartus II software Assignment Editor.

You must set the V_{CCIO} to 2.5 V when OCT R_D is used for the LVDS input buffer, even if the LVDS input buffer is powered by V_{CCPD}.

Table 7–11. On-Chip Differential Termination in Quartus II Software Assignment Editor

Assignment Name	Allowed Values	Applies To
Input Termination (Accepts wildcards/groups)	Parallel 50 Ω with calibration	Input buffers for single-ended and differential-HSTL/SSTL standards
	Differential	Input buffers for LVDS receivers on row I/O banks.
Output Termination	Series 25 Ω without calibration	Output buffers for single-ended LVTTL/LVCMOS and HSTL/SSTL standards as well as differential HSTL/SSTL standards.
	Series 50 Ω without calibration	
	Series 25 Ω with calibration	
	Series 40 Ω with calibration	
	Series 50 Ω with calibration	
	Series 60 Ω with calibration	

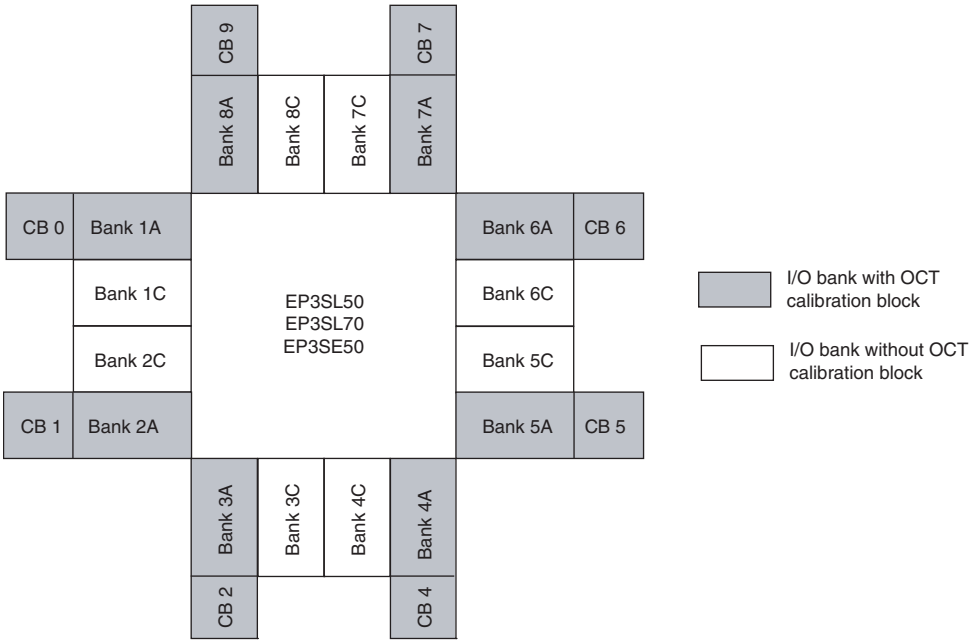
OCT Calibration

Stratix III devices support calibrated OCT R_S and calibrated OCT R_T on all I/O pins. You can calibrate the Stratix III I/O bank with any of eight OCT calibration blocks in EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SE50, EP3SE80, and EP3SE110 devices and ten OCT calibration blocks in EP3SL200, EP3SE260, and EP3SL340 devices.

OCT Calibration Block Location

Figure 7–13, Figure 7–14, and Figure 7–15 show the location of OCT calibration blocks in Stratix III devices.

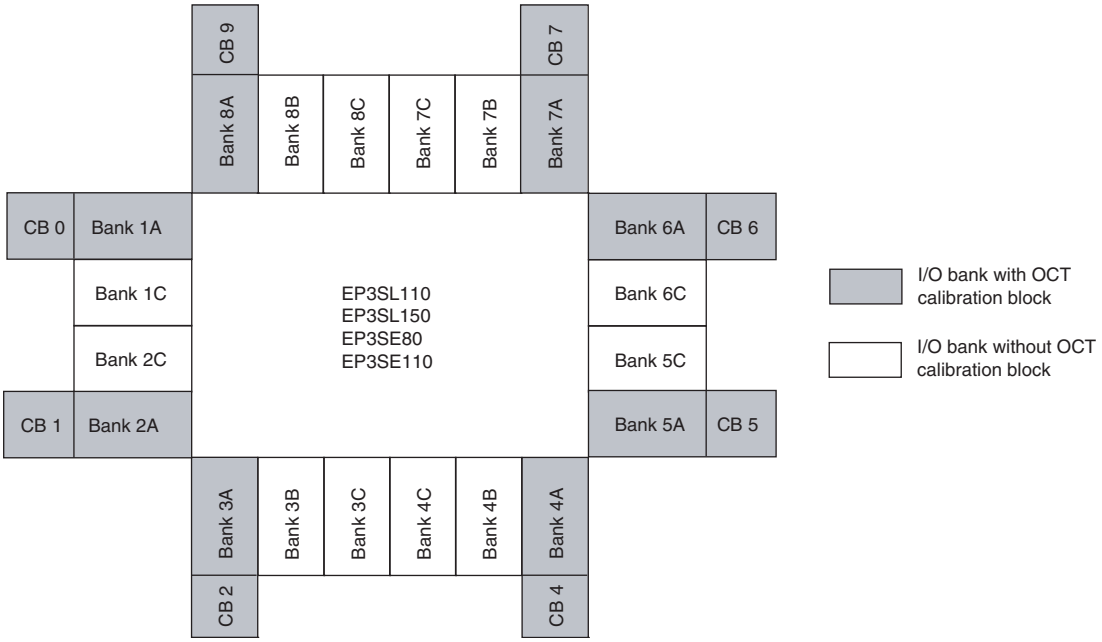
Figure 7–13. OCT Calibration Block (CB) Location in EP3SL50, EP3SL70, and EP3SE50 Devices *(Note 1)*



Note to Figure 7–13:

(1) Figure 7–13 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

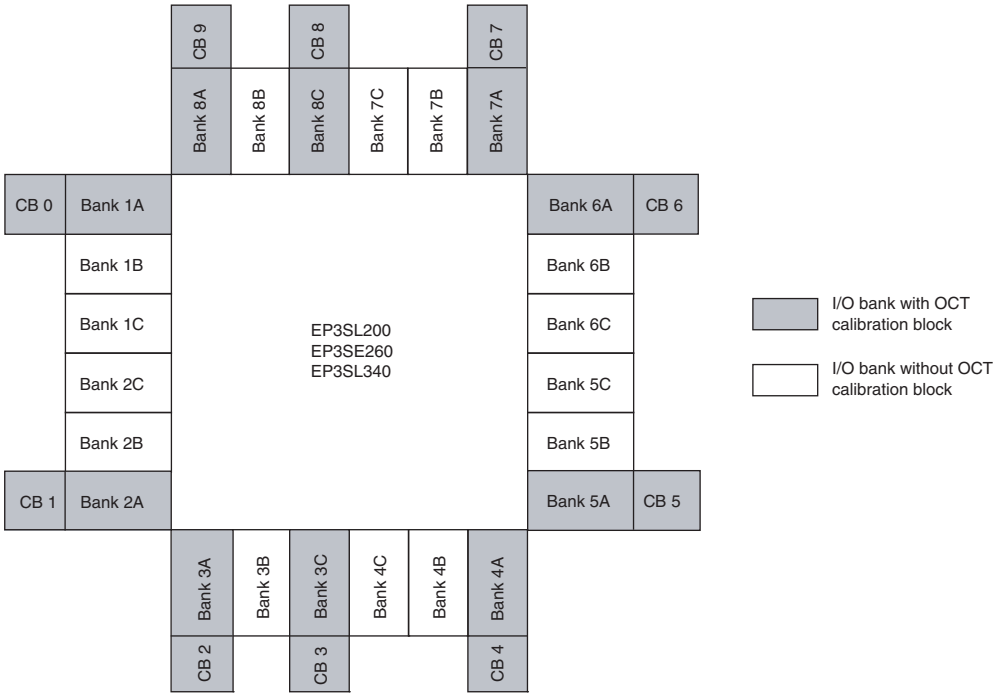
Figure 7–14. OCT Calibration Block (CB) Location in EP3SL110, EP3SL150, EP3SE80, and EP3SE110 Devices *(Note 1)*



Note to Figure 7–14:

(1) Figure 7–14 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Figure 7–15. OCT Calibration Block (CB) Location in EP3SL200, EP3SE260 and EP3SL340 *(Note 1)*



Note to Figure 7–15:

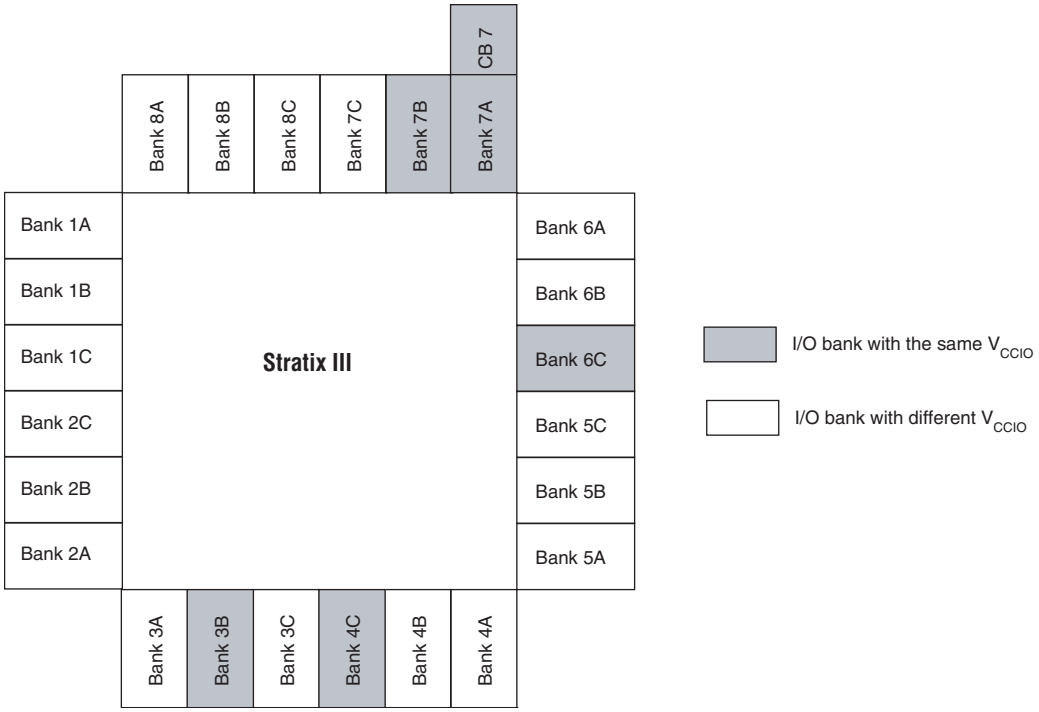
(1) Figure 7–15 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Sharing an OCT Calibration Block in Multiple I/O Banks

An OCT calibration block has the same V_{CCIO} as the I/O bank that contains the block. OCT R_S calibration is supported on all I/O banks with different V_{CCIO} voltage standards, up to the number of available OCT calibration blocks. You can configure I/O banks to receive calibrated codes from any OCT calibration block with the same V_{CCIO}. All I/O banks with the same V_{CCIO} can share one OCT calibration block, even if that particular I/O bank has an OCT calibration block.

For example, Figure 7–16 shows a group of I/O banks that have the same V_{CCIO} voltage. If a group of I/O banks have the same V_{CCIO} voltage, you can use one OCT calibration block to calibrate the group of I/O banks placed around the periphery. Because 3B, 4C, 6C, and 7B have the same V_{CCIO} as bank 7A, you can calibrate all four I/O banks (3B, 4C, 6C, and 7B) with the OCT calibration block located in bank 7A. You can enable this by serially shifting out OCT R_S calibration codes from the OCT calibration block located in bank 7A to the I/O banks located around the periphery.

Figure 7–16. Example of Sharing Multiple I/O Banks with One OCT Calibration Block *(Note 1)*



Note to Figure 7–16:

(1) Figure 7–16 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

OCT Calibration Block Modes of Operation

Stratix III devices support calibration OCT R_S and OCT R_T in all I/O banks. The calibration can occur in either power-up mode or user mode.

Power-Up Mode

In power-up mode, OCT calibration is automatically performed at power up and calibrated codes are shifted to selected I/O buffers before transitioning to user mode.

User Mode

During user mode, OCTUSRCLK, ENAOCT, nCLRUSR, and ENASER[9..0] signals are used to calibrate and serially transfer calibrated codes from each OCT calibration block to any I/O. Table 7–12 lists the user controlled calibration block signal names and their descriptions.

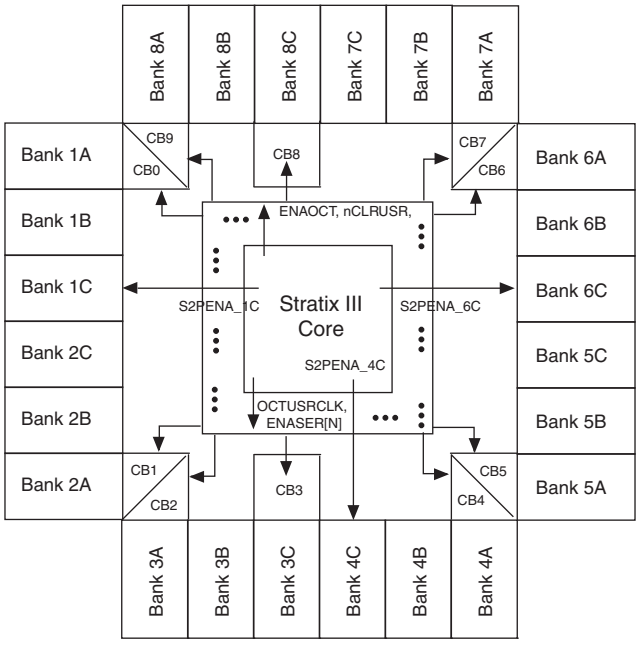
Table 7–12. OCT Calibration Block Ports for User Control and Description

Signal Name	Description
OCTUSRCLK	Clock for OCT block.
ENAOCT	Enable OCT Termination (generated by user IP).
ENASER[9..0]	When ENAOCT = 0, each signal enables the OCT serializer for the corresponding OCT calibration block. When ENAOCT = 1, each signal enables OCT calibration for the corresponding OCT calibration block.
S2PENA_<*bank#*>	Serial-to-parallel load enable per I/O bank.
nCLRUSR	Clear user.

Figure 7–17 shows the flow of the user signal. When ENAOCT is 1, all OCT calibration blocks are in calibration mode, and when ENAOCT is 0, all OCT calibration blocks are in serial data transfer mode. The OCTUSRCLK clock frequency must be 20 MHz or less.

You must generate all user signals on the rising edge of OCTUSRCLK.

Figure 7–17. Signals Used for User Mode Calibration *(Note 1)*



Note to Figure 7–17:

(1) Figure 7–17 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

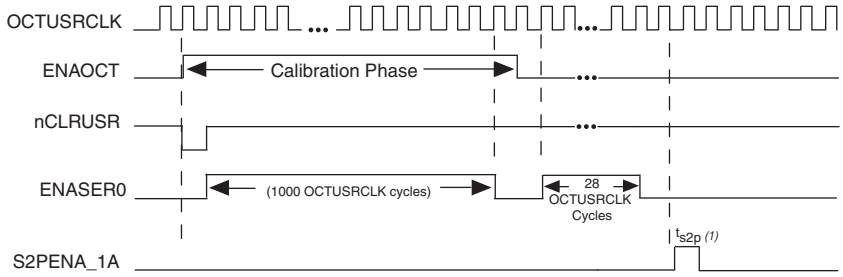
OCT Calibration

Figure 7–18 shows the user-mode signal-timing waveforms. To calibrate OCT block[N] (where N is a calibration block number), you must assert ENAOCT one cycle before asserting ENASER[N]. Also, nCLRUSR must be set to low for one OCTUSRCLK cycle before ENASER[N] signal is asserted. An asserted ENASER[N] signals for 1000 OCTUSRCLK cycles to perform $OCTR_S$ and $OCTR_T$ calibration. ENAOCT can be deasserted one clock cycle after the last ENASER is deasserted.

Serial Data Transfer

When calibration is complete, you must serially shift out the 28-bit OCT calibration code (14-bit OCT RS code and 14-bit OCT RT) from each OCT calibration block to the corresponding I/O buffers. Only one OCT calibration block can send out the codes at any given time by asserting only one ENASER[N] signal at a time. After ENAOCT is deasserted, you must wait at least 1 OCTUSRCLK cycle to enable any ENASER[N] signal to begin serial transfer. To shift 28-bit code from OCT calibration block[N], ENASER[N] must be asserted for exactly 28 OCTUSRCLK cycles. There must be at least one OCTUSRCLK cycle gap between two consecutive asserted ENASER signals. For these requirements, refer to Figure 7–18.

Figure 7–18. OCT User-Mode Signal Timing Waveform for One OCT Block



Note to Figure 7–18:

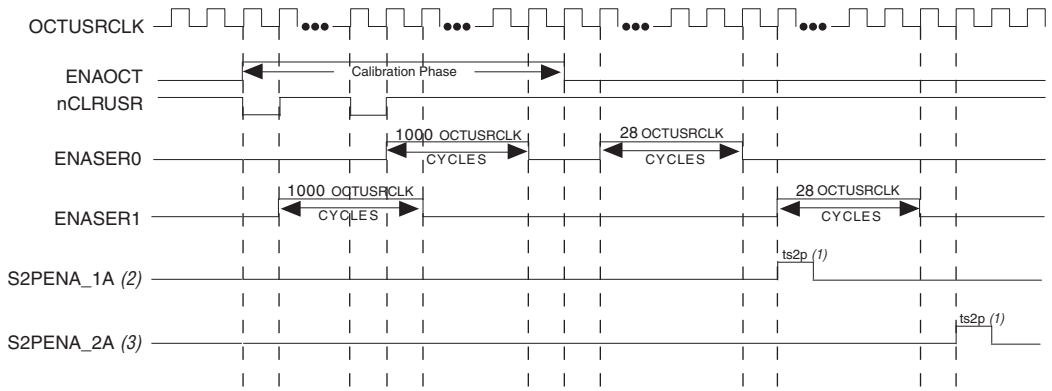
(1) ts2p ≥ 25 ns

After calibrated codes are shifted serially to the corresponding I/O buffers, they must be converted from serial format to parallel format before being used in the I/O buffers. Figure 7–18 shows S2PENA signals that can be asserted at any time to update the calibration codes in each I/O bank. All I/O banks that received the codes from the same OCT calibration block can have S2PENA asserted at the same time, or at a different time, even while another OCT calibration block is calibrating and serially shifting codes. The S2PENA signal is asserted one OCTUSRCLK cycle after ENASER is deasserted for at least 25 ns. You cannot use I/Os for transmitting or receiving data when their S2PENA is asserted for parallel codes transfer.

Example of Using Multiple OCT Calibration Blocks

Figure 7–19 shows a signal timing waveform for two OCT calibration blocks doing R_S and R_T calibration. Calibration blocks can start calibrating at different times by asserting ENASER signals at different times. ENAOCT must stay asserted while any calibration is ongoing. nCLRUSR must be set to low for one OCTUSRCLK cycle before each ENASER[N] signal is asserted. In Figure 7–19, when nCLRUSR is set to 0 for the second time to initialize OCT calibration block 0, this does not affect OCT calibration block 1, whose calibration is already in progress.

Figure 7–19. OCT User-Mode Signal Timing Waveform for Two OCT Blocks



Notes to Figure 7–19:

(1) ts2p ≥ 25 ns

(2) S2PENA_1A is asserted in Bank 1A for calibration block 0.

(3) S2PENA_2A is asserted in Bank 2A for calibration block 1.

RS Calibration

If only RS calibration is used for an OCT calibration block, its corresponding ENASER signal must be asserted for 240 OCTUSRCLK cycles for calibration.

You still have to assert the ENASER signal for 28 OCTUSRCLK cycles for serial transfer.

For more information, refer to the *ALT_OCT Megafunction User Guide* and *AN 465: Implementing OCT Calibration in Stratix III Devices*.

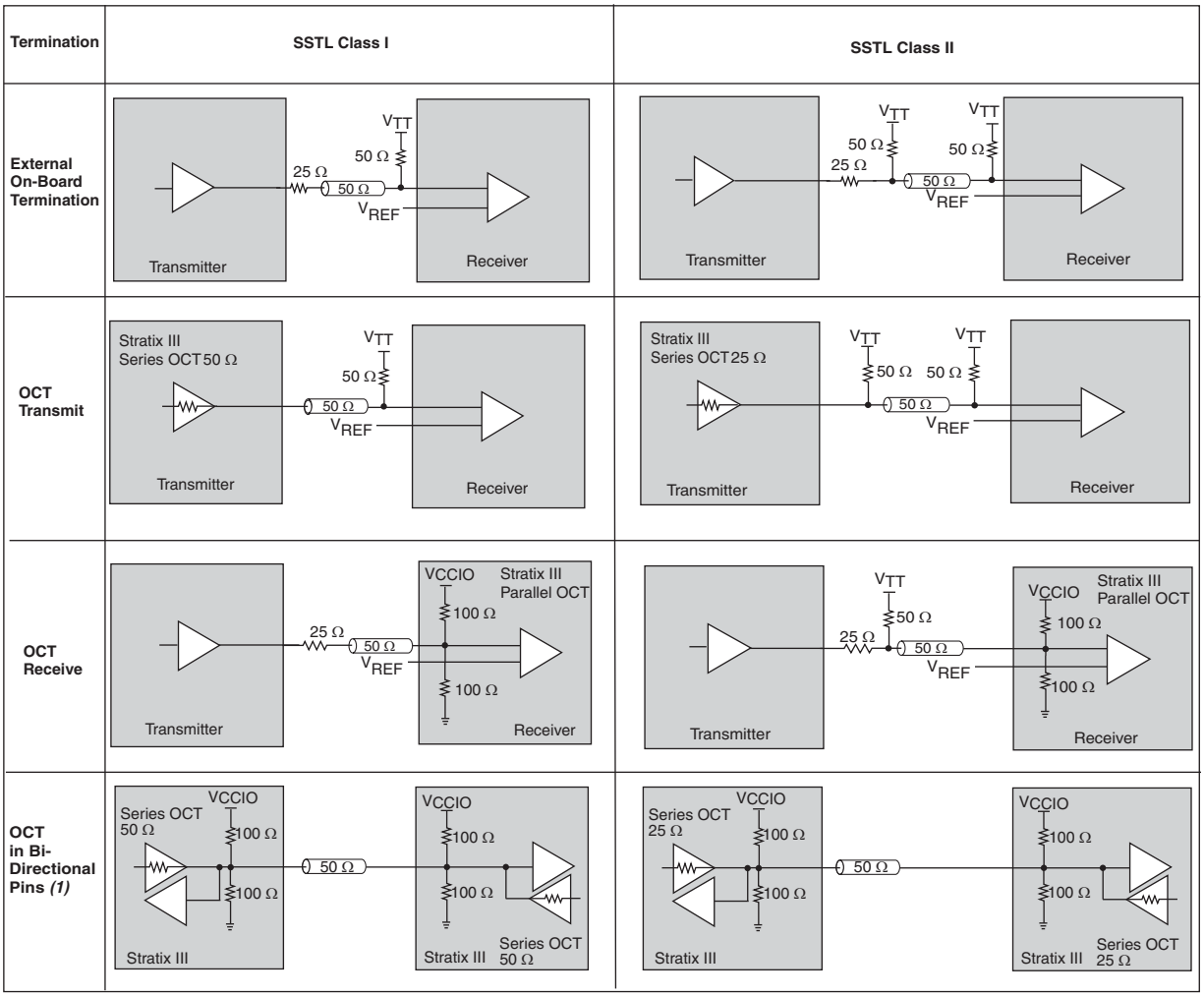
Termination Schemes for I/O Standards

The following section describes the different termination schemes for the I/O standards used in Stratix III devices.

Single-Ended I/O Standards Termination

Voltage-referenced I/O standards require both an input reference voltage, V_{REF}, and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device. Figure 7–20 and Figure 7–21 show the details of SSTL and HSTL I/O termination on Stratix III devices.

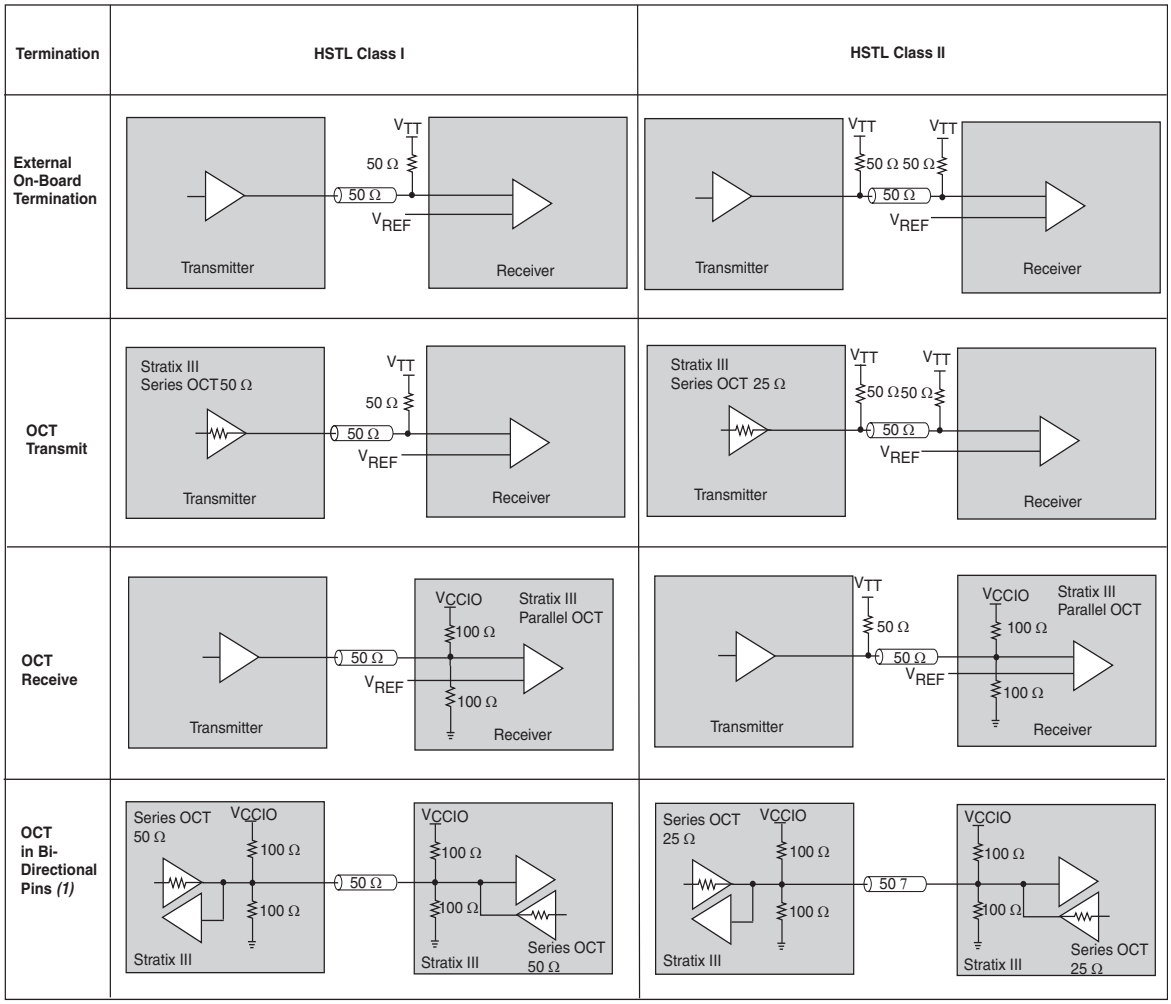
Figure 7–20. SSTL I/O Standard Termination for Stratix III Devices



Note to Figure 7–20:

(1) In Stratix III devices, series and parallel OCT cannot be used simultaneously. For more information, refer to "Dynamic OCT" on page 7–25.

Figure 7–21. HSTL I/O Standard Termination for Stratix III Devices



Note to Figure 7–21:

(1) In Stratix III devices, you cannot use simultaneously series and parallel OCT. For more information, refer to "Dynamic OCT" on page 7–25.

Differential I/O Standards Termination

Stratix III devices support differential SSTL-2 and SSTL-18, differential HSTL-18, HSTL-15, HSTL-12, LVDS, LVPECL, RSDS, and mini-LVDS. Figure 7–22 through Figure 7–28 show the details of various differential I/O termination on Stratix III devices.

Differential HSTL and SSTL outputs are not true differential outputs. They use two single-ended outputs with the second output programmed as inverted.

Figure 7–22. Differential SSTL I/O Standard Termination for Stratix III Devices

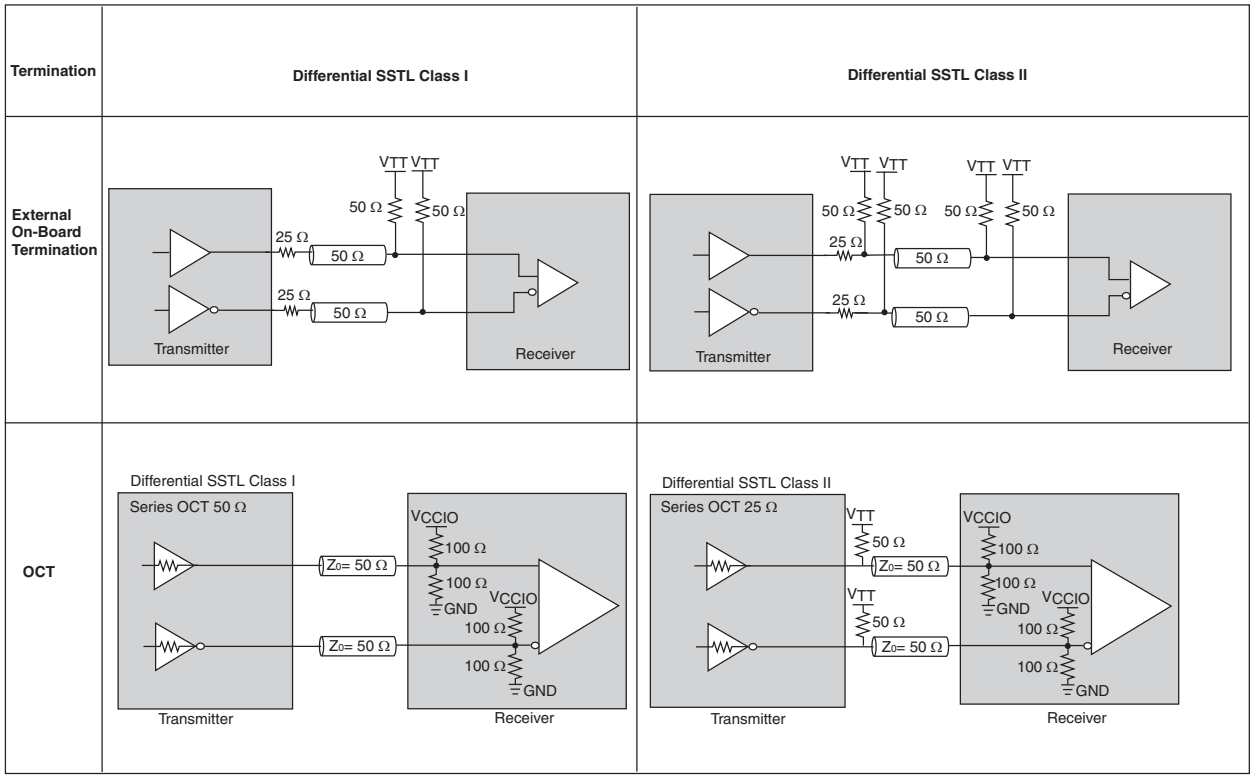
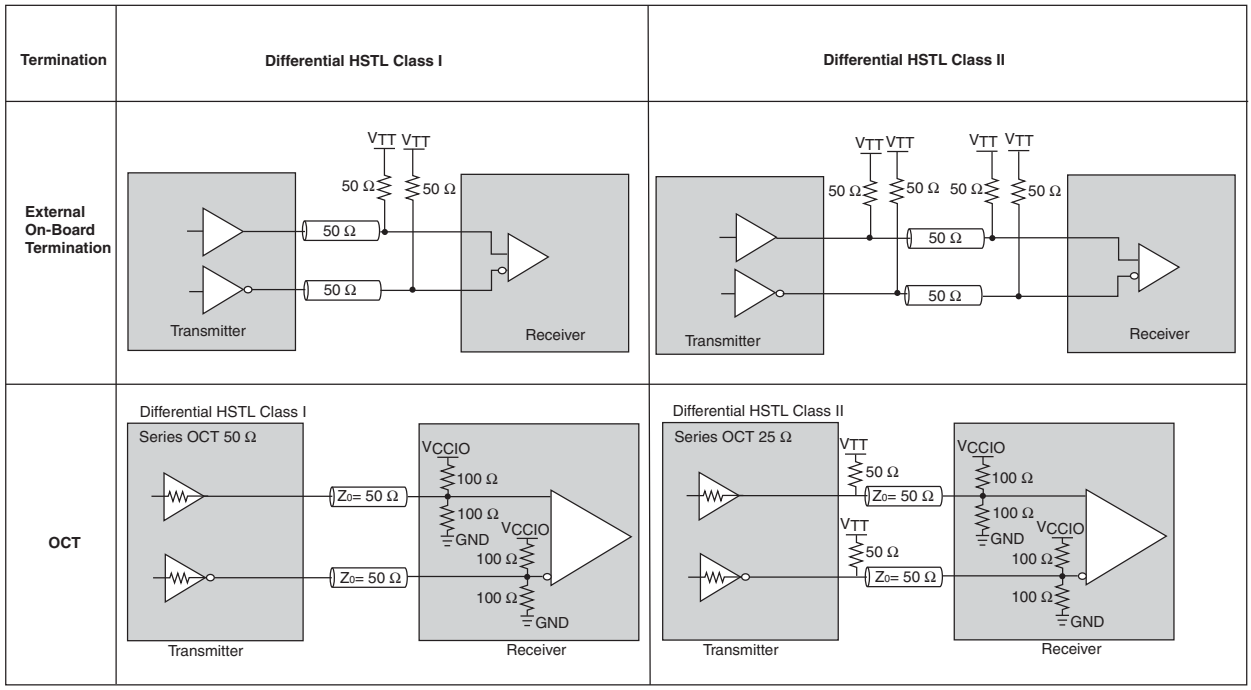


Figure 7–23. Differential HSTL I/O Standard Termination for Stratix III Devices

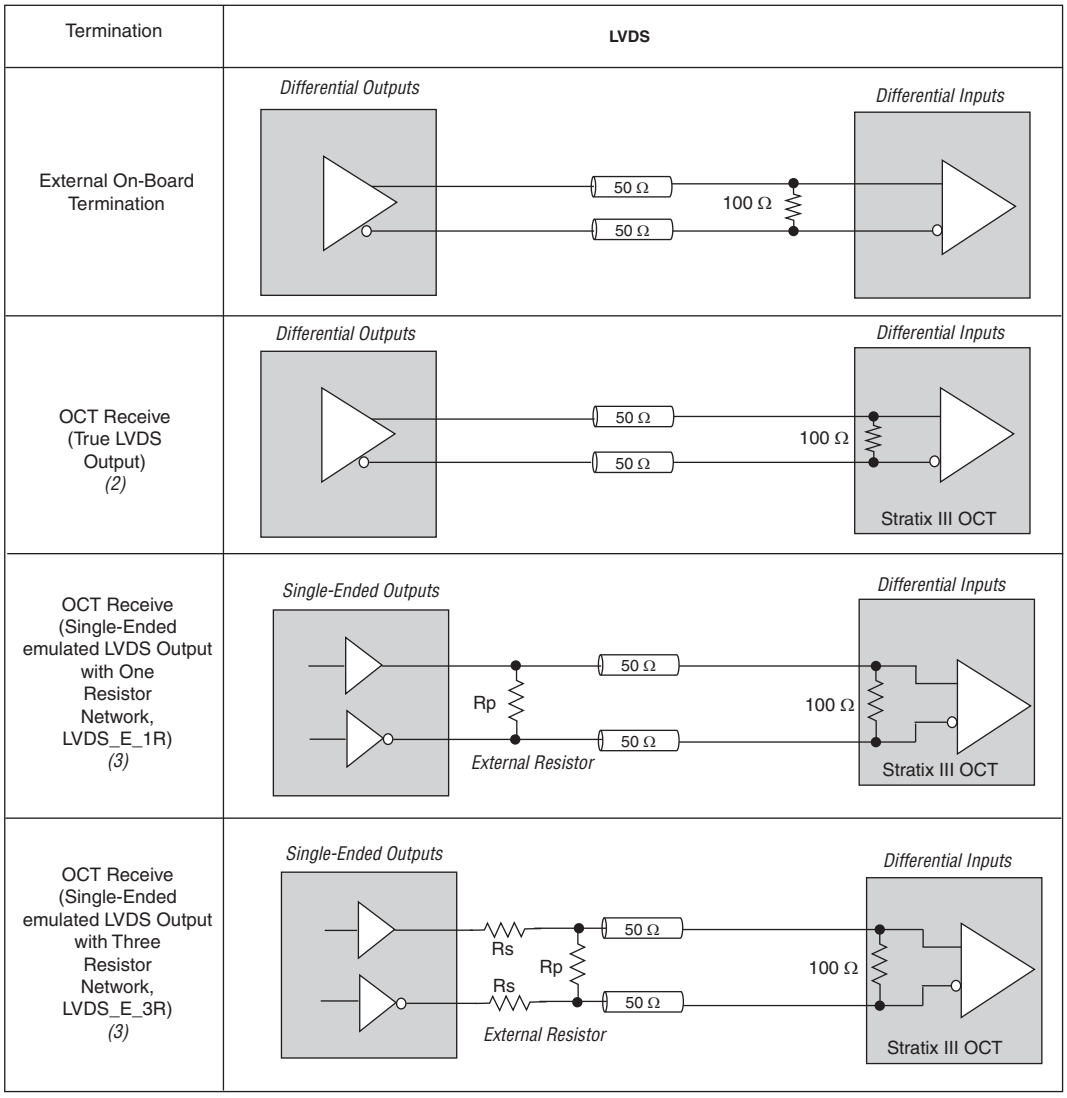


LVDS

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. In Stratix III devices, the LVDS I/O standard requires a 2.5-V V_{CCIO} level. The LVDS input buffer requires 2.5-V V_{CCPD}. Use this standard in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. LVDS requires a 100-Ω termination resistor between the two signals at the input buffer. Stratix III devices provide an optional 100-Ω differential termination resistor in the device using on-chip differential termination.

Figure 7–24 shows the details of LVDS termination. The OCT R_D is only available in row I/O banks.

Figure 7–24. LVDS I/O Standard Termination for Stratix III Devices *(Note 1)*



Notes to Figure 7–24:

(1) R_P=120 Ω for LVDS_E_1R, R_P=170 Ω, and R_S=120 Ω for LVDS_E_3R.

(2) Row I/O banks support true LVDS output buffers.

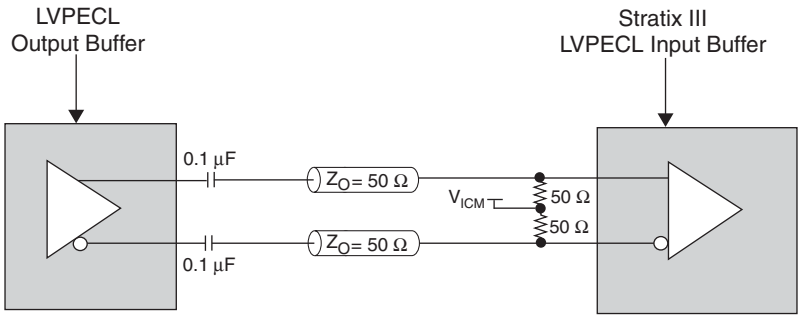
(3) Column and row I/O banks support LVDS_E_1R and LVDS_E_3R I/O standards using two single-ended output buffers.

Differential LVPECL

In Stratix III devices, the LVPECL I/O standard is supported on input clock pins on column and row I/O banks. LVPECL output operation is not supported by Stratix III devices. LVDS input buffers are used to support LVPECL input operation. AC coupling is required when LVPECL common mode voltage of the output buffer is higher than Stratix III LVPECL input common mode voltage. Figure 7–25 shows the AC coupled termination scheme. The 50-Ω resistors used at the receiver end are external to the device.

DC-coupled LVPECL is supported if the driving device's LVPECL output common mode voltage is within the Stratix III LVPECL input buffer specification (see Figure 7–26).

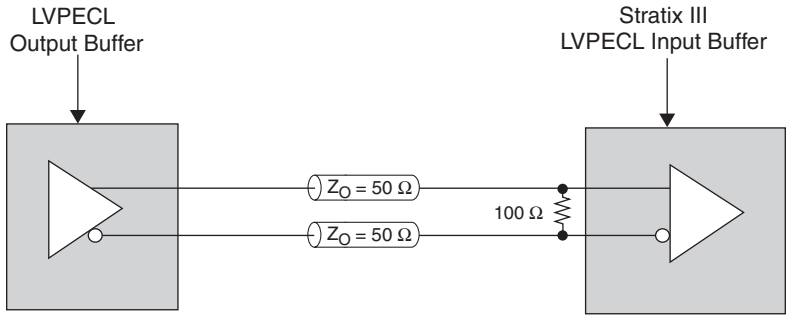
Figure 7–25. LVPECL AC Coupled Termination *(Note 1)*



Note to Figure 7–25:

(1) The LVPECL AC-coupled termination is applicable only when an Altera FPGA LVPECL transmitter is used.

Figure 7–26. LVPECL DC Coupled Termination *(Note 1)*



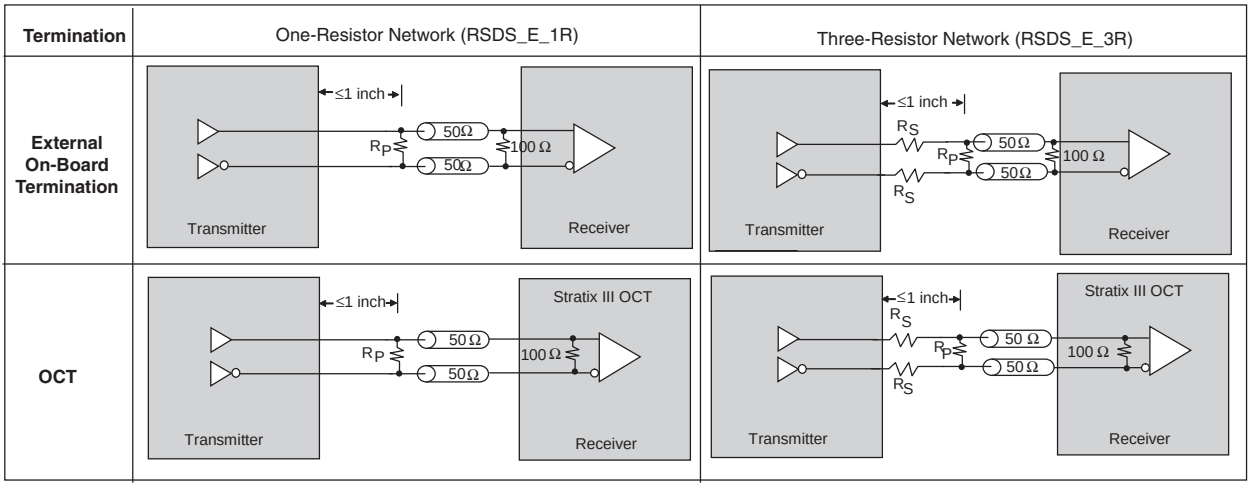
Note to Figure 7–26:

(1) The LVPECL DC-coupled termination is applicable only when an Altera FPGA LVPECL transmitter is used.

RSDS

The row I/O banks support RSDS output using true LVDS output buffers without an external resistor network. The column I/O banks support RSDS output using two single-ended output buffers with the external one- or three-resistor networks, as shown in Figure 7–27.

Figure 7–27. RSDS I/O Standard Termination for Stratix III Devices *(Note 1), (2)*



Notes to Figure 7–27:

(1) R_P=120 Ω for RSDS_E_1R, R_P=170 Ω, and R_S=120 Ω for RSDS_E_3R.

(2) Column and row I/O banks support RSDS_E_1R and RSDS_E_3R I/O standards using two single-ended output buffers.

A resistor network is required to attenuate the LVDS output-voltage swing to meet the RSDS specifications. You can modify the three-resistor network values to reduce power or improve the noise margin. The resistor values chosen should satisfy Equation 7–1:

Equation 7–1.

$$\frac{Rs \times \frac{Rp}{2}}{Rs + \frac{Rp}{2}} = 50\Omega$$

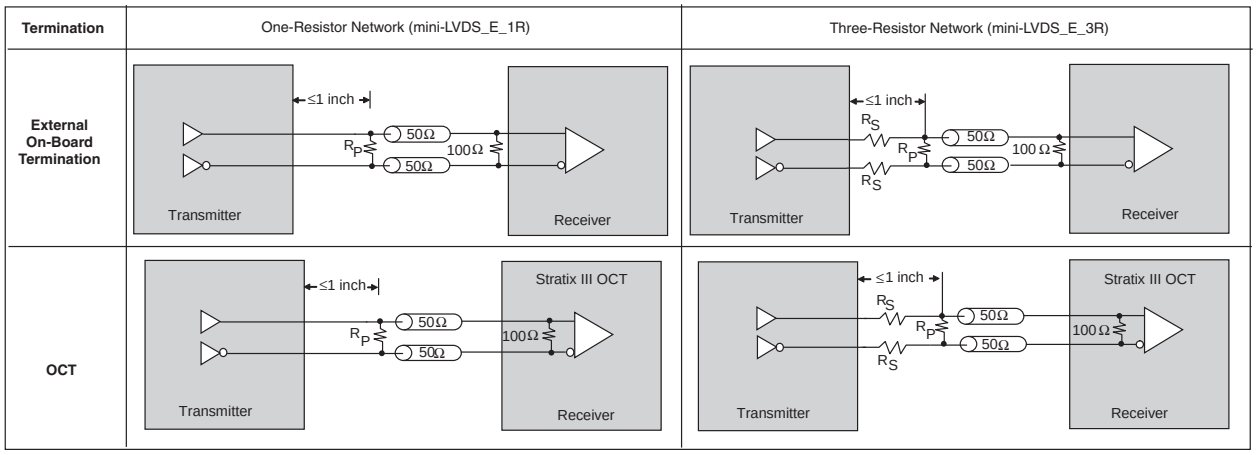
Altera recommends that you perform additional simulations using IBIS models to validate that custom resistor values meet the RSDS requirements.

For more information about the RSDS I/O standard, refer to the *RSDS Specification* from the National Semiconductor website.

Mini-LVDS

The row I/O banks support mini-LVDS output using true LVDS output buffers without an external resistor network. The column I/O banks support mini-LVDS output using two single-ended output buffers with the external one- or three-resistor network, as shown in Figure 7–28.

Figure 7–28. Mini-LVDS I/O Standard Termination for Stratix III Devices *(Note 1)*, *(2)*



Notes to Figure 7–28:

(1) R_P=120 Ω for mini-LVDS_E_1R, R_P=170 Ω, and R_S=120 Ω for mini-LVDS_E_3R.

(2) Column and row I/O banks support mini-LVDS_E_1R and mini-LVDS_E_3R I/O standards using two single-ended output buffers.

A resistor network is required to attenuate the LVDS output voltage swing to meet the mini-LVDS specifications. You can modify the three-resistor network values to reduce power or improve the noise margin. The resistor values chosen should satisfy Equation 7–2:

Equation 7–2.

$$\frac{Rs \times \frac{Rp}{2}}{Rs + \frac{Rp}{2}} = 50\Omega$$

Altera recommends that you perform additional simulations using IBIS models to validate that custom resistor values meet the RSDS requirements.

For more information about the mini-LVDS I/O standard, refer to the *mini-LVDS Specification* from the Texas Instruments website.

Design Considerations

While Stratix III devices feature various I/O capabilities for high-performance and high-speed system designs, there are several other considerations that require attention to ensure the success of those designs.

I/O Termination

I/O termination requirements for single-ended and differential I/O standards are discussed in this section.

Single-Ended I/O Standards

Although single-ended, non-voltage-referenced I/O standards do not require termination, impedance matching may be necessary to reduce reflections and improve signal integrity.

Voltage-referenced I/O standards require both an input reference voltage, $V_{REF,}$ and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device. Each voltage-referenced I/O standard requires a unique termination setup. For example, a proper resistive signal termination scheme is critical in SSTL2 standards to produce a reliable DDR memory system with superior noise margin.

Stratix III OCT R_S and OCT R_T provide the convenience of no external components. Alternatively, you can use external pull-up resistors to terminate the voltage-referenced I/O standards, such as SSTL and HSTL.

Differential I/O Standards

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the signal line. Stratix III devices provide an optional differential on-chip resistor when using LVDS.

For PCB layout guidelines, refer to *AN 224: High-Speed Board Layout Guidelines* and *AN 315: Guidelines for Designing High-Speed FPGA PCBs*.

I/O Banks Restrictions

Each I/O bank can simultaneously support multiple I/O standards. The following sections provide guidelines for mixing non-voltage-referenced and voltage-referenced I/O standards in Stratix III devices.

Non-Voltage-Referenced Standards

Each Stratix III device I/O bank has its own V_{CCIO} pins and supports only one V_{CCIO}, either 1.2, 1.5, 1.8, 2.5, 3.0, or 3.3 V. An I/O bank can simultaneously support any number of input signals with different I/O standard assignments, as listed in Table 7–2.

For output signals, a single I/O bank supports non-voltage-referenced output signals that are driving at the same voltage as V_{CCIO}. Since an I/O bank can only have one V_{CCIO} value, it can only drive out that one value for non-voltage-referenced signals. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V standard inputs and outputs and 3-V LVCMOS inputs (not output or bi-directional pins).

Voltage-Referenced Standards

To accommodate voltage-referenced I/O standards, each Stratix III device I/O bank has one VREF pin feeding a common V_{REF} bus. If it is not used as a VREF pin, it cannot be used as a generic I/O pin and should be tied to V_{CCIO} or GND. Each bank can only have a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time.

An I/O bank featuring single-ended or differential standards can support voltage-referenced standards as long as all voltage-referenced standards use the same V_{REF} setting.

For performance reasons, voltage-referenced input standards use their own V_{CCPD} level as the power source. This feature allows you to place voltage-referenced input signals in an I/O bank with a V_{CCIO} of 2.5 or below. For example, you can place HSTL-15 input pins in an I/O bank with a 2.5-V V_{CCIO}. However, voltage-referenced input with parallel OCT enabled requires the V_{CCIO} of the I/O bank to match the voltage of the input standard.

Voltage-referenced bi-directional and output signals must be the same as the I/O bank's V_{CCIO} voltage. For example, you can only place SSTL-2 output pins in an I/O bank with a 2.5-V V_{CCIO}.

Mixing Voltage-Referenced and Non-Voltage-Referenced Standards

An I/O bank can support both non-voltage-referenced and voltage-referenced pins by applying each of the rule sets individually. For example, an I/O bank can support SSTL-18 inputs and 1.8-V inputs and outputs with a 1.8-V V_{CCIO} and a 0.9-V V_{REF}. Similarly, an I/O bank can support 1.5-V standards, 1.8-V inputs (but not outputs), and HSTL and HSTL-15 I/O standards with a 1.5-V V_{CCIO} and 0.75-V V_{REF}.

For pin connection guidelines, refer to the *Stratix III Device Family Pin Connection Guidelines*.

Chapter Revision History

Table 7–13 lists the revision history for this chapter.

Table 7–13. Chapter Revision History (Part 1 of 2)

Date and Revision	Version	Changes Made
July 2010	1.9	■ Updated Figure 7–25, Figure 7–26, and Figure 7–28. ■ Updated Equation 7–1 and Equation 7–2.
March 2010	1.8	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated "Programmable Pull-Up Resistor" section. ■ Updated Figure 7–2, Figure 7–3, Figure 7–4, Figure 7–5, Figure 7–6. ■ Updated Table 7–2, Table 7–3, and Table 7–7. ■ Added reference before Table 7–11. ■ Removed "Conclusion" section. ■ Minor text edit.
May 2009	1.7	■ Updated "Expanded On-Chip Series Termination with Calibration" and "Mixing Voltage-Referenced and Non-Voltage-Referenced Standards" sections. ■ Added "Left Shift Series Termination Control" section. ■ Updated Table 7–8 and Table 7–9. ■ Updated Figure 7–24.
February 2009	1.6	■ Updated Table 7–3, Table 7–7, Table 7–8, and Table 7–11. ■ Updated Figure 7–2, Figure 7–3, Figure 7–4, Figure 7–5, and Figure 7–6. ■ Updated "LVDS Input On-Chip Termination (R_D)" section. ■ Removed "Referenced Documents" section.
October 2008	1.5	Text, Table, and Figure updates: ■ Updated Table 7–2, Table 7–4, Table 7–7, and Table 7–10. ■ Updated notes for Table 7–2. ■ Updated notes for Figure 7–3, Figure 7–4, Figure 7–5, Figure 7–6, and Figure 7–7. ■ Updated "Stratix III I/O Banks", "Modular I/O Banks", "High-Speed Differential I/O with DPA Support", "Dynamic On-Chip Termination", "LVDS Input On-Chip Termination (RD)", "Serial Data Transfer", "LVDS", "RSDS", "mini-LVDS", "Voltage-Referenced Standards", "Stratix III I/O Banks", "MultiVolt I/O Interface", and "On-Chip Parallel Termination with Calibration" sections. ■ Updated Figure 7–1. ■ Added Table 7–3. ■ Updated New Document Format.

Table 7–13. Chapter Revision History (Part 2 of 2)

Date and Revision	Version	Changes Made
May 2008	1.4	Text, Table, and Figure updates: ■ Updated Table 7–2 headers and notes. ■ Updated Figure 7–1. ■ Updated "Programmable Slew Rate Control", "Programmable Pre-Emphasis", "LVDS Input On-Chip Termination (RD)", and "Programmable Differential Output Voltage". ■ Added Note (1) for Figure 7–17. ■ Updated notes for Figure 7–24. ■ Added Note (2) for Figure 7–27. ■ Added Note (2) for Figure 7–28.
November 2007	1.3	Figure updates: ■ Updated Figure 7–4, Figure 7–5, Figure 7–6, Figure 7–15, and Figure 7–16. ■ Updated Note (1) of Figure 7–25.
October 2007	1.2	Text changes, figure updates, removal of a section: ■ Minor text edits to second to last paragraph on pg 7-47. ■ Updated Table 7–2, Table 7–4, Table 7–5, Table 7–8. ■ Updated "Introduction", "OCT Calibration Block Modes of Operation", "Power Up Mode", "User Mode". ■ Changed 3.0-V LVTTL and 3.0-V LVCMOS to be 3.3/3.0-V LVTTL and 3.3/3.0-V LVCMOS throughout the document. ■ Added a note to Figure 7–1, Figure 7–3, Figure 7–4, Figure 7–5, Figure 7–6, Figure 7–7, Figure 7–14, Figure 7–15, Figure 7–16, and Figure 7–17. ■ Updated Figure 7–8, Figure 7–18, Figure 7–22, Figure 7–23, Figure 7–25, Figure 7–28, and Figure 7–29. ■ Added Figure 7–18 and Figure 7–20. ■ Expanded "3.3-V I/O Interface" on page 7–15 to include new information. ■ Removed section "OCT Calibration Block Architecture", "OCT Calibration Block Ports", and "OCT Calibration Block Code Data Transfer". ■ Added section "OCT Calibration", "Serial Data Transfer", "Example of Using Multiple OCT Calibration Blocks", "RS Calibration", and "Referenced Documents." ■ Added live links for references.
May 2007	1.1	■ Added the feature programmable input delay to "Stratix III I/O Structure" on page 7–13. ■ Updated Table 7–4 and Table 7–7. ■ Updated "LVDS Input On-Chip Termination (RD)" on page 7–29. ■ Updated Figure 7–3 through Figure 7–7. ■ Updated Figure 7–23, Figure 7–24. ■ Minor text edits to page 14.
November 2006	1.0	Initial Release.